RGM-R-2010

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

ELECTRONICS AND COMMUNICATION ENGINEERING

Affiliated to JNTU-Anantapur, Approved by AICTE-New Delhi, Accredited by NBA-New Delhi

NANDYAL-518 501, KURNOOL Dist., A.P.

EMBEDDED SYSTEMS

ACADEMIC REGULATIONS,
COURSE STRUCTURE AND SYLLABI

APPLICABLE FOR STUDENTS ADMITTED INTO

M.TECH (REGULAR) FROM 2010-11

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REGULATIONS

For pursuing Two year Master (post graduate) Degree of study in Engineering (M.Tech), offered by Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal-518501 under Autonomous status and herein referred to as RGMCET (Autonomous)

All the rules specified herein approved by the Academic Council will be in force and applicable to students admitted from the Academic Year 2010-11 onwards. Any reference to "Institute" or "College" in these rules and regulations stands for Rajeev Gandhi Memorial College of Engineering and Technology (Autonomous).

All the rules and regulations, specified here after shall be read as a whole for the purpose of interpretation as and when a doubt arises , the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, Rajeev Gandhi Memorial College of Engineering and Technology shall be the Chairman, Academic Council.

I. ACADEMIC REGULATIONS 2010 FOR M.TECH (REGULAR)

(Effective for the students admitted into first year from the Academic Year 2010-2011)

THE M.TECH DEGREE OF JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, ANANTAPUR, SHALL BE CONFERRED ON CANDIDATES WHO ARE ADMITTED TO THE M.TECH PROGRAM AT RGMCET, NANDYAL AND THEY SHALL FULFIL ALL THE REQUIREMENTS FOR THE AWARD OF THE DEGREE.

1.0 Eligibility for Admissions:

Admission to the above program shall be made subject to the eligibility, qualifications and specialization prescribed by Andhra Pradesh State Council of Higher Education (APSCHE) from time to time.

Admissions shall be made on the basis of merit rank obtained in GATE examination or PGCET conducted by any University of Andhra Pradesh designated by Govt. of A.P., or on the basis of any other order of merit prescribed by APSCHE, subject to the reservations prescribed by the Government of A.P. from time to time.

2.0 Award of M.Tech Degree:

2.1) The student shall be declared eligible for the award of the M.Tech degree, if he pursues a course of study and completes it successfully for not less than prescribed course work duration and not more than double the prescribed course work duration.

2.2) The student, who fails to fulfil all the academic requirements for the award of the degree within double the course work duration from the year of his admission, shall forfeit his seat in M.Tech course.

2.2) The minimum clear instruction days for each semester shall be 95.

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3.0 Courses of Study:

The following specializations are offered at present for the M.Tech course of study.

1. Computer Science (CSE)
2. Digital Systems and Computer Electronics (ECE)
3. Embedded Systems (ECE)
4. Machine Design (ME)
5. Power Electronics (EEE)
6. Software Engineering (IT)

and any other course as approved by the appropriate authorities from time to time.

4.0 Course pattern:

4.1) The entire course of study is of four semesters. During the first and second semesters the student has to undergo course work and during the third and fourth semesters the student has to carry out project work.

4.2) The student eligible to appear for the End Examination in a subject, but absent at it or has failed in the End Examination may appear for that subject at the supplementary examination.

TABLE 1: CREDITS

	SEMESTER			
	Periods/ Week	Credits	Internal Marks	External Marks
Theory	04	04	40	60
Practical	03	02	40	60
Seminar		02	100	
Comprehensive Viva-voce		04		100
Project		12		

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TABLE: 2 COURSE PATTERN

Semester	No.of Subjects	Number of Labs	Total Credits	
First	06	02	6X4=24 2X2=04	28
Second	06	02 Comprehensive Viva	6X4=24 2X2=04 1X4=04	32
Third	Seminar(3rd semester) Project Work			02
Fourth				12
Total credits				74

5.0 Attendance:

5.1) The candidate shall be deemed to have eligibility to write end semester examinations if he has secured a minimum of 75% of attendance in aggregate of all the subjects.

5.2) Condonation of shortage of attendance up to 10% i.e. 65% and above and below 75% may be given by the College academic committee consisting of Principal, Head of the Department and a senior faculty member.

5.3) Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence.

5.4) **Shortage of attendance below 65% shall in no case be condoned**.

5.5) The candidate shall not be promoted to the next semester unless he fulfils the attendance requirements of the previous semester.

6.0 Evaluation:

The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks for Theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

6.1) For the theory subjects 60 marks shall be for the External End Examination, While 40 marks shall be for Internal Evaluation, based on the better of the marks secured in the two Mid Term-Examinations held, one in the middle of the Semester (I-IV units) and another immediately After the completion of instruction (V-VIII) units with four questions to be answered out of six, evaluated for 40 marks. Each question carries 10 marks. Each midterm examination shall be conducted for duration of 120 minutes. The End Examination will have 08 questions and 5 questions are to be answered and each question carries 12 marks.

6.2) For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks shall be for Internal evaluation based on the day-to-day performance. End practical examinations for M.Tech courses will be conducted with two Examiners, one of them being Laboratory Class Teacher and second Examiner shall be external from other institution.

6.3) Student has to undergo a comprehensive viva pertaining to his specialization which carries 100 marks. He has to secure 50% marks to obtain required credits. Comprehensive viva will be held at the end of II semester with HOD, senior faculty member and external Examiner from outside the institute. For this, HOD of the Department shall submit a panel of 5 Examiners, who are eminent in that field. One from the panel will be selected by the principal of the institute as external Examiner for comprehensive viva.

6.4) For Seminar100 marks shall be for Internal evaluation. The candidate has to secure a minimum of 50 marks to be declared successful. The assessment will be made by a board consisting of HOD and two Internal experts at the end of III semester.

6.5) The candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Examination and Internal evaluation taken together.

6.6) In case the candidate does not secure the minimum academic requirement in any subject(as specified in 6.5.) he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the course when next offered or do any other specified subject as may be required.

7.0 Re-registration for improvement of Internal marks:

Following are the conditions to avail the benefit of improvement of internal marks.

7.1) The candidate should have completed the course work and obtained examinations results for I & II semesters.

7.2) He should have passed all the subjects for which the internal marks secured are more than 50%.

7.3) Out of the subjects the candidate has failed in the examination due to lack of Internal marks secured being less than 50%, the candidate shall be given one chance for Theory subject and subject to a maximum of three Theory subjects.

7.4) The candidate has to re-register for the chosen subjects and fulfil the academic requirements as and when they are offered.

7.5) For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of the Principal, RGMCET payable at RGMCET Nandyal branch along with the requisition through the HOD of the respective Department.

7.6) In case of availing the Improvement of Internal marks, the Internal marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

8.0 Evaluation of Project / Dissertation work :

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Department.

8.1) Registration of Project work: The candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Sem).

8.2) An Internal Department Committee (I.D.C) consisting of HOD, Supervisor and One Internal senior expert shall monitor the progress of the project work.

8.3) The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

8.4) The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.

8.5) The candidate shall be allowed to submit the thesis / dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva voce examination of the project. The viva voce examination may be conducted once in two months for all the candidates submitted during that period.

8.6) Three copies of the Thesis / Dissertation certified in the prescribed form by the supervisor & HOD shall be submitted to the institute.

8.7) The Department shall submit a panel of three experts for a maximum of 5 students at a time. However, the thesis / dissertation will be adjudicated by the board consists of HOD, concerned supervisor and one external Examiner from other institute nominated by the principal from a panel of Examiners submitted by the Department to the Controller of Examinations.

8.8) If the report of the board is favourable in viva voce examination, the board shall jointly report candidates work as:

1. Satisfactory
2. Not satisfactory

If the report of the viva voce is not satisfactory the candidate will retake the viva voce examination after three months. If he fails to get a satisfactory report at the second viva voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the thesis.

9.0 Award of Degree and Class:

After the student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following classes:

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TABLE 3: AWARD OF DIVISION

Class Awarded	% of marks to be secured	From the aggregate marks secured form the 74 Credits.
First Class with Distinction	70% and above	
First Class	Below 70% but not less than 60%	
Second Class	Below 60% but not less than 50%	

(The marks in Internal evaluation and End Examination shall be shown separately in the marks memorandum)

10.0 Supplementary Examinations:

Apart from the regular End Examinations the institute may also schedule and conduct supplementary examinations for all subjects for the benefit of students with backlogs. Such of the students writing supplementary examinations as supplementary candidates may have to write more than one examination per day.

11.0 Transcripts:

After successful completion of prerequisite credits for the award of degree a Transcript containing performance of all academic years will be issued as a final record. Duplicate transcripts will also be issued if required after the payment of requisite fee and also as per norms in vogue.

12.0 Minimum Instruction Days:

The minimum instruction days for each semester shall be 95 clear instruction days excluding the days allotted for tests/examinations and preparation holidays declared if any.

13.0 Amendment of Regulations:

The college may, from time to time, revise, amend or change the regulations, scheme of examinations and syllabi. However the academic regulations of any student will be same throughout the course of study in which the student has been admitted.

14.0 Transfers

There shall be no branch transfers after the completion of admission process.

15.0 With holding of results:

If the candidate has not paid any dues to the institute or if any case of in-discipline is pending against him, the result of the candidate will be with held and he will not be allowed for the next semester. The issue of the degree is liable to be withheld in such cases.

16.0 Transitory Regulations:

Candidates who have discontinued or have been detained for want of attendance are eligible for admission to the same or equivalent subjects as and when subjects are offered, subject to 6.5 and 2.0

17.0 Rules of Discipline:

17.1) Any attempt by any student to influence the teachers, Examiners, faculty and staff of controller of Examination for undue favours in the exams, and bribing them either for marks or attendance will be treated as malpractice cases and the student can be debarred from the college.

17.2) When The student absents himself, he is treated as to have appeared and obtained zero marks in that subject(s) and grading is done accordingly.

17.3) When the performance of the student in any subject(s) is cancelled as a punishment for indiscipline, he is awarded zero marks in that subject(s).

17.4) When the student's answer book is confiscated for any kind of attempted or suspected malpractice the decision of the Examiner is final.

18.0 General:

18.1) The Academic Regulation should be read as a whole for the purpose of any interpretation.

18.2) In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the College Academic Council is final.

18.3) The Institute may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Institute.

18.4) Where the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".

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EMBEDDED SYSTEMS

COURSE STRUCTURE

I M.TECH, I-SEMESTER

Code	Subject	Scheme of instruction periods/week		Credits	Scheme of Examination		
		Theory	Practical		Internal	External	Total
D0602101	Embedded System Concepts	4		4	40	60	100
D0603101	Advanced Computer Architecture	4		4	40	60	100
D5501101	Advanced DSP and Applications	4		4	40	60	100
D5502101	Micro Controllers & Interfacing	4		4	40	60	100
D5503101	Operating Systems	4		4	40	60	100
	ELECTIVE-I	4		4	40	60	100
D0607101	Expert Systems						
D5504101	VLSI Technology						
D5505101	Algorithms for VLSI Design Automation						
D5591101	Micro Controllers and Interfacing Lab		3	2	40	60	100
D5592101	FPGA/CPLD Lab		3	2	40	60	100
	Total	**24**	**6**	**28**	**320**	**480**	**800**

I M.TECH, II-SEMESTER

Code	Subject	Scheme of instruction periods/week		Credits	Scheme of Examination		
		Theory	Practical		Internal	External	Total
D5506102	Embedded System Design	4		4	40	60	100
D5507102	Real Time Operating Systems	4		4	40	60	100
D5508102	Hardware Software Co-design	4		4	40	60	100
D0615102	FPGA Architecture & Applications	4		4	40	60	100
D5509102	CMOS Digital IC Design	4		4	40	60	100
	ELECTIVE-II	4		4	40	60	100
D0605101	Digital Design Through Verilog						
D5510102	Low Power VLSI Design						
D0608101	Network Security and Cryptography						
	LABORATORY						
D5592102	Real Time Operating Systems Lab		3	2	40	60	100
D5593102	CMOS Digital IC Design Lab		3	2	40	60	100
D5594102	Comprehensive Viva			4		100	100
	Total	**24**	**6**	**32**	**320**	**580**	**900**

II M.TECH, III-SEMESTER & IV-SEMESTER

Code	Subject	Credits	Internal	External	Total
D5595103	Seminar (End of III Semester)	2	100	-	100
D5596104	Project work	12	-	-	-
	Total	**14**	**100**	**-**	**100**

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M.Tech I-Sem (Embedded Systems) **T** **C**

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(D0602101) EMBEDDED SYSTEM CONCEPTS

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems.

UNIT II

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT III

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space.

UNIT IV

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique.

UNIT V

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes.

UNIT VI

INSTRUCTION SETS: Introduction, preliminaries, ARM processor, SHARC processor.

UNIT VII

SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications, system analysis and architecture design.

UNIT VIII

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes, etc.

TEXT BOOKS:

1) Computers as a component: principles of embedded computing system design- wayne wolf
2) An embedded software premier: David E. Simon
3) Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1) Embedded real time systems programming-Sri ram V Iyer, pankaj gupta, TMH, 2004.
2) Embedded system design- A unified hardware/software introduction- frank vahid, tony D. Givargis, John
Willey, 2002.

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M.Tech I-Sem (Embedded Systems) **T** **C**

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(D0603101) ADVANCED COMPUTER ARCHITECTURE

UNIT I

FUNDAMENTALS OF COMPUTER DESIGN: Technology trends, cost- measuring and reporting performance quantitative principles of computer design.

UNIT II

INSTRUCTION SET PRINCIPLES AND EXAMPLES: Classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set- instructions for control flow- encoding an instruction set.-the role of compiler.

UNIT III

INSTRUCTION LEVEL PARALLELISM (ILP): Overcoming data hazards, reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP.

UNIT IV

ILP SOFTWARE APPROACH: Compiler Techniques, Static Branch Protection, VLIW Approach, H.W support for more ILP at compile time- H.W verses S.W solutions.

UNIT V

MEMORY HIERARCHY DESIGN: Cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

UNIT VI

MULTIPROCESSORS AND THREAD LEVEL PARALLELISM: Symmetric shared memory architectures, distributed shared memory, Synchronization, multi threading.

UNIT VII

STORAGE SYSTEMS: Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

UNIT VIII

INTER CONNECTION NETWORKS AND CLUSTERS: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster.

TEXT BOOKS:

1) John. Hennessy & David A. Patterson Morgan Kufmann, ”Computer Architecture A quantitative approach”, 3rd edition (An Imprint of Elsevier).

REFERENCES:

1) Kai Hwang and A. Briggs, “Computer Architecture and parallel Processing”, International Edition McGraw-Hill.
2) Dezso Sima, Terence Fountain, Peter Kacsuk, “Advanced Computer Architectures”, Pearson.

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M.Tech I-Sem (Embedded Systems) **T** **C**

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(D5501101) ADVANCED DSP & APPLICATIONS

UNIT I

LTI DISCRETE-TIME SYSTEMS IN THE TRANSFORM DOMAIN: Types of Linear-Phase transfer functions, Complementary Transfer Functions, Inverse Systems, System identification, Digital Two-Pairs.

UNIT II

DIGITAL FILTER STRUCTURE AND DESIGN: All pass filters, Tunable IIR Digital filter, IIR & FIR tapped Cascaded Lattice Structures, Parallel All pass realization of IIR Transfer Functions, Digital Sine-Cosine generator.

UNIT III

Computational Complexity of Digital filter Structures, Design of IIR filter using pade' approximation, Least square design methods, Design of computationally efficient FIR filters.

UNIT IV

DSP ALGORITHMS: FFT, Sliding Discrete Fourier transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNIT V

ANALYSIS OF FINITE WORD LENGTH EFFECTS: The Quantization Process and errors, Quantization of fixed-point Numbers, Analysis of Coefficient quantization effects, A/D conversion Noise Analysis, Analysis of Arithmetic Round of errors.

UNIT VI

ADAPTIVE FILTERS: FIR adaptive filters - Adaptive filter based on steepest descent method - Widrow-Hoff LMS adaptive algorithms, normalized LMS. Adaptive channel equalization - adaptive echo cancellation - Adaptive noise cancellation - Adaptive recursive (IIR) filters. RLS adaptive filters - Exponentially weighted RLS - Sliding window RLS.

UNIT VII

APPLICATIONS OF DIGITAL SIGNAL PROCESSING: Dual Tone Multi-frequency Signal Detection, Spectral Analysis of Sinusoidal Signals, Spectral Analysis of Nonstationary Signals, Musical Sound Processing, Over Sampling A/D Converter, Over Sampling D/A Converter.

UNIT VIII

DSP PROCESSORS: Applications, architecture , Addressing modes ,instruction set of TMS 320 C54XX Processors , simple programmes.

TEXT BOOKS:

1) Digital Signal Processing by Sanjit K Mitra, Tata MCgraw Hill Publications.
2) Digital Signal Processing Principles, Algorithms,Applications By J G Proakis, D G.Manolokis,PHI.Discrete-Time Signal Processing by A V Oppenhiem, R W Schafer, Pearson Education Asia.
3) Digital signal processors by avtar singh & S.Srinivasan,.Thomson publications.
4) Adaptive filter theory by Simon Haykin, Pearson education.
5) Statistical and adaptive Signal Processing by Dimitris G.Manolakis and Vinay K.Ingle.

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REFERENCES:

1) Naim Dahnoun, "Digital Signal Processing Implementation Using the TMS320C6000 DSP Platform", 1st Edition.
2) T.J. Terrel and Lik-Kwan Shark, "Digital Signal Processing-A Student Guide", 1st Edition, MACMILLAN PRESS Ltd.
3) David J Defatta J, Lucas Joseph G & Hodkiss William S, "Digital Signal Processing: A System Design Approach", 1st Edition, John Wiley.
4) Rulph Chassaing, "DSP Applications using 'C' and the TMS320C6X DSK", 1st Edition.
5) Andrew Bateman, Warren Yates, "Digital Signal Processing Design", 1st Edition.
6) John G Proakis, Dimitris G Manolakis, "Introduction to Digital Signal Processing", 1st Edition.
7) Kreig Marven & Gillian Ewers, "A Simple approach to Digital Signal processing", 1st Edition, Wiely Interscience.
8) JAMES H. McClellan, Ronald Schaffer and Mark A. Yoder, "DSP FIRST - A Multimedia Approach", 1st Edition, Prentice Hall.
9) Oppenheim A.V and Schafer R.W, "Digital Signal Processing", 1st Edition, PH.

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M.Tech I-Sem (Embedded Systems) | **T** | **C**
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(D5502101) MICRO CONTROLLERS & INTERFACING

UNIT I

INTEL 8051: Architecture of 8051, Memory Organization, Register banks, Bit addressing media, SFR area, addressing modes, Instruction set, Programming examples.

UNIT II

8051 Interrupt structure, Timer modules, Serial Features, Port structure, Power saving modes.

UNIT III

MOTOROLA 68HC11: Controllers features, Different modes of operation and memory map, Functions of I/O ports in single chip and expanded multiplexed mode, Timer system.

UNIT IV

Input capture, Output compare and pulsed accumulator features of 68HC11, Serial peripherals, Serial Communication interface, Analog to digital conversion features.

UNIT V

PIC MICROCONTROLLERS: Program memory, CPU registers, Register file structure, Block diagram of PIC 16C74, I/O ports. Timer 0,1 and 2 features, Interrupt logic, serial peripheral interface, I^2C bus, ADC, UART, PIC family parts.

UNIT VI

MICROCONTROLLER INTERFACING: 8051, 68HC11, PIC-16C6X and External Memory Interfacing – Memory Management Unit, Instruction and data cache, memory controller. On Chip Counters, Timers, Serial I/O, Interrupts and their use. PWM, Watch dog, ISP, IAP features.

UNIT VII

INTERRUPT SYNCHRONIZATION: Interrupt vectors & priority, external interrupt design. Serial I/O DevicesRS232 Specifications, RS422/Apple Talk/ RS 423/RS435 & other communication protocols. Serial Communication Controller.

UNIT VIII

CASE STUDIES: Design of Embedded Systems using the micro controller 8051, 68HC11, PIC-16C6X for applications in the area of Communications, Automotives, industrial control.

TEXT BOOKS:

1) M.A. Mazadi & J.G. Mazidi, "The 8051 Micro Controller & Embedded Systems", Pearson Education. Asia (2000).
2) John B. Peatman, Designing with PIC Micro Controllers, Pearson Education.
3) Jonathan W. Valvano, Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning, 1999.

REFERENCES:

1) 8-bit Embedded Controllers, INTEL Corporation 1990.
2) John B.Peatman, "Designing with PIC Microcontrollers", Pearson Education Inc, India, 2005.

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M.Tech I-Sem (Embedded Systems) **T C**

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(D5503101) OPERATING SYSTEMS

UNIT I

INTRODUCTION: Operating system definition, Objective and functions, types, different parts, Structure of operating system, trends- parallel computing, distributed computing; Open systems, Hardware, software, firmware.

UNIT II

PROCESS SCHEDULING: Definition of a process; process states, transitions, process control, suspend and process, interrupt processing, nucleus of an operating system; parallel processing; Mutual exclusion, Critical Section; Solution of mutual exclusion; Semaphores; Deadlock- occurrence, prevention, detection and recovery.

UNIT III

STORAGE MANAGEMENT: Storage organization, management strategies, hierarchy; virtual storage, paging, segmentation.

UNIT IV

FILE SYSTEM MANAGEMENT: File system (function of a file system)- data hierarchy, blocking and buffering, file organization, queued and basic access methods, backup and recovery.

UNIT V

I/O MANAGEMENT: (functions of I/O management subsystem), Distributed computing- OSI view, OSI network management, MAP, TOP, GOSIP, TCP/IP.

UNIT VI

OS SECURITY: Requirements, external security, operational security, surveillance, threat monitoring; Introduction to Cryptography.

UNIT VII

CASE STUDIES: UNIX- Shell, Kernel, File System, Process Management, Memory Management, I/O System, Distributed UNIX.

UNIT VIII

CASE STUDIES: Example of operating system-MS-DOS, Windows, OS/2, Apple Macintosh & Linux.

TEXT BOOKS:

1) Dietal H.M "An Introduction to OS" Pearson Education Pvt. Ltd/PHI New Delhi, 12th Indian Reprint 2003.

2) Andrew S.Tanenbaum, "Modern OS"PHI Pearson Education Pvt. Ltd New Delhi, 3rd Indian Reprint 2004.

3) Silberschatz A, Galvin. P and Gagne. G, "Operating System Concepts", John Wiley and Sons. Singapore, 2002.

REFERENCES:

1) William Stallings, "Operating Systems", Pearson Education Pvt. Ltd.

2) D.M. Dhamdhere, "Operating Systems – A Concept Approach", Tata McGraw Hill, 2003.

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M.Tech I-Sem (Embedded Systems) **T** **C**

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(D0607101) EXPERT SYSTEMS

(ELECTIVE - I)

UNIT I

KNOWLEDGE REPRESENTATION AND ISSUES: Notational systems: Trees, graphs, hierarchies, propositional and predicate logics, frames, semantics networks, constraints, conceptual dependencies, database, knowledge discovery in databases (KDD).

UNIT II

SEARCH: State-space representations, Depth-first, breadth-first, heuristic search, Planning and game playing, Genetic algorithms.

UNIT III

LOGICAL REASONING AND PROBABILISTIC REASONING: Predicate, Calculus resolution, completeness, and strategies, Unification, Prolog, monotonic and non-monotonic reasoning.

UNIT IV

Probabilistic inference networks, Fuzzy inference rules, Bayesian rules. Dempster-Shafer Calculus.

UNIT V

LEARNING AND COMMON SENSANE REASONING: Robot actions, strips, triangle tables, case based reasoning, spatial and temporal formalisms.

UNIT VI

Knowledge acquisition, classification rules, self directed systems.

UNIT VII

NEURAL NETWORKS: Principles, biological analogies, Training (techniques and errors), Recognition.

UNIT VIII

EXPERT SYSTEMS Expert Systems, Organization, tools, limits, examples.

TEXT BOOKS:

1. Charniak .E,And McDermott .D., ”Intoduction to Artificial intelligence”, Adiison-Wesley, 1987
2. Giarratano.J.,And Riley G., ”Expert Systems principles an Programming” PWS-KENT,1989

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(D5504101) VLSI TECHNOLOGY

(ELECTIVE I)

UNIT I

INTRODUCTION TO MOS TECHNOLOGY: Overview of VLSI Design Methodologies**,** VLSI Design flow, Styles of VLSI Design, CAD Technology, MOS Transistors and its Trends.

UNIT II

BASIC ELECTRICAL PROPERTIES OF MOS: I_{ds}-V_{ds} Relationships, Threshold voltage V_t, g_m, g_{ds} and W_o, Pass Transistor, MOS Z_{pu}/Z_{pd}, MOS Transistor circuit model.

UNIT III

CMOS Design: CMOS Logic, CMOS Gate Design, Transmission Gate Logic Design, Bi-CMOS Inverters, Latch-up in CMOS circuits.

UNIT IV

LAYOUT DESIGN AND TOOLS: Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

UNIT V

LOGIC GATES & LAYOUTS: Static Complementary Gates, Switch Logic, Alternative Gate Circuits, Low Power Gates, Resistive and Inductive Interconnect Delays.

UNIT VI

COMBINATIONAL LOGIC NETWORKS: Layouts, Simulation, Network Delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT VII

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT VIII

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, High level Synthesis, Architecture for Low Power, SOCs and Embedded CPU Architecture Testing.

TEXT BOOKS:

1. K. Eshraghian etal.(3 authors), "Essentials of VLSI Circuits and Systems", PHI of India Ltd., 2005
2. Wayne Wolf, "Modern VLSI Design", 3/E, Pearson Education, fifth Indian Reprint, 2005.
3. Sung-Mo Kang and Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design" TATA McGraw HILL Edition

REFERENCES:

1. N.H.E Weste, K.Eshraghian, "Principals of CMOS Design", Addison Wesley, 2nd Edition.
2. Ken Martin, "Digital Integrated Circuits Design" oxford University Press.

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(D5505101) ALGORITHMS FOR VLSI DESIGN AUTOMATION

(ELECTIVE I)

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

UNIT IV

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT V

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis.

UNIT VI

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT VII

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and routing for segmented and staggered Models.

UNIT VIII

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1) S.H.Gerez, "Algorithms for VLSI Design Automation", Wiley Student Edition, John Wiley & Sons (Asia) Pvt. Ltd., 1999.
2) Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd edition, Springer International Edition, 2005.

REFERENCES:

1) Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", Wiley, 1993.
2) Wayne Wolf, "Modern VLSI Design: Systems on silicon", Pearson Education Asia, 2nd Edition,1998.

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(D5591101) MICROCONTROLLERS & INTERFACING LAB

ASSEMBLY:

1) Write a program to a) Clear the Register and b) Add 3 to Register Ten Times and Place the Result into Memory Use the Indirect Instructions to Perform Looping.

PROGRAMING IN C:

2) A Door Sensor is connected to RB1 Pin and a Buzzer is connected to RB7**.** Write a Program to monitor Door Sensor and when it Open, Sounds the Buzzer by sending a Square Wave of few Hundred Hz Frequency to it.
3) Write a Program to Toggle all the Bits of PORT B parts continuously with a 250ns Delay.
4) Stepper Motor Control using Microcontroller.

Use Microcontrollers for the following Experiments.

INTERFACING:

5) Elevator Interface.
6) Key Board Interface.
7) LED Interface.
8) Temperature Sensor.
9) SORT RTO'S on to 89c51 Board.
10) Sample the Signal using ADC and Reconstruct by using DAC.

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3 **2**

(D5592101) FPGA/CPLD LAB

1. Simulation and Verification of Logic Gates.
2. Simulation and Verification of 74x138.
3. Simulation and Verification of 74x151.
4. Simulation and Verification of 74x157.
5. Simulation and Verification of 74x280.
6. Simulation and Verification of 74x382.
7. Simulation and Verification of 74x74.
8. Simulation and Verification of 74x163.
9. Simulation and Verification of 74x194.
10. Design, Simulation of Counters- Ring Counter, Johnson Counter, Mod counters.
11. Finite State Machine- Mealy and Moore Machines.
12. Design, Simulation and verification of Dual Priority encoder.
13. Design, Simulation and verification of Floating point encoder.
14. Design, Simulation and verification of Error correcting code with hamming code.

Implementation of all the Design using FPGA and CPLD Devices.

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4 **4**

(D5506102) EMBEDDED SYSTEMS DESIGN

UNIT I

Embedded Design Life Cycle: Introduction, Product Specification, Hardware/software partitioning, Iteration and Implementation, Detailed hardware and software design, Hardware/Software integration, Product Testing and Release, Maintaining and upgrading existing products.

UNIT II

Selection Process: Packaging the Silicon, Adequate Performance, RTOS Availability, Tool chain Availability, Other issues in the Selection process, partitioning decision: Hardware/Software Duality, Hardware Trends, ASICs and Revision Costs.

UNIT III

Development Environment: The Execution Environment, Memory Organization, System Startup. Special Software Techniques: Manipulating the Hardware, Interrupts and Interrupt service Routines (ISRs), Watchdog Times, Flash Memory, Design Methodology. Basic Tool Set: Host – Based Debugging, Remote Debuggers and Debug Kernels, ROM Emulator, Logic Analyzer.

UNIT IV

BDM: Background Debug Mode, Joint Test Action Group (JTAG) and Nexus. ICE – Integrated Solution: Bullet Proof Run Control, Real time trac, Hardware Break points, Overlay memory, Timing Constrains, Usage Issue, Setting the Trigger.

UNIT V

Testing: Why Test? When to Test? Which Test? When to Stop? Choosing Test cases, Testing Embedded Software, Performance Testing Maintenance and Testing, The Future.

UNIT VI

Writing Software for Embedded Systems: The compilation Process, Native Versus Cross-Compilers, Runtime Libraries, Writing a Library, Using alternative Libraries, using a standard Library.

UNIT VII

Emulation and debugging techniques: Debugging techniques, The role of the development system.

UNIT VIII

Buffering and Other Data Structures: What is a buffer? Linear Buffers, Directional Buffers, Double Buffering, Buffer Exchange, Linked Lists, FIFOs, Circular Buffers, Buffer Under run and Overrun, Allocating Buffer Memory.

TEXTBOOKS

1. Embedded System Design – Introduction to Processes, Tools, Techniques, Arnold S Burger, CMP Books
2. Embedded Systems Design by Steve Heath, Newnes.

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(D5507102) REAL TIME OPERATING SYSTEMS

UNIT-I

Real Time operating systems: Architecture of kernel, Tasks and Task scheduler, interrupt services routines, semaphores, mutex, mailboxes, message queues, event register, pipes, signals, timers, memory management, priority inversion problem.

UNIT-II

REAL TIME APPLICATIONS: Digital control, High level controls, signal processing, other real time applications.

UNIT-III

HARD VERSUS SOFT REAL TIME SYSTEMS: Jobs and processors, release times, deadlines, and timing constraints. Hard and soft timing constraints. Hard real time systems, soft real time systems.

UNIT-IV

REAL TIME SCHEDULING APPROACHES: Clock Driven, Weighted round robin, priority driven, dynamic vs static systems, effective release times an dead lines.

UNIT-V

REAL TIME OPERATING SYSTEM: QNX Neutrino, VX works, Microc/os-II, RT Linux ,overview of unix/Linux.

UNIT-VI

SHELL AND SYSEM PROGRAMMING: Shell programming-shell variables, shell programming constructs, processes, signals, multithreading, semaphores, mutex, shared memory, messagequeue.

UNIT-VII

PROGRAMMING IN RT LINUX: Overview of RT Linux, core RT Linux API, semaphore management, mutex management.

UNIT-VIII

FAULT TOLERANCE TECHNIQUES: Introduction, fault causes, Types, detection, Fault and error containment, Hardware, software and timing redundancy

TEXTBOOKS

1) Embedded Real Time Systems-Blackbook Dr.k.v.k.k.Prasad
2) Jane W.S.Liu,"Real Time Systems",McGraw.Hill
3) C.M.Krishna,KANG G.Shin,"Real Time Systems",pearson edition.

REFERENCES

1) www.kernel.org
2) Vxworks Programming Guide.

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(D5508102) HARDWARE SOFTWARE CO- DESIGN

UNIT I

CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

UNIT II

HARDWARE/SOFTWARE CO- SYNTHESIS ALGORITHMS: Introduction, preliminaries, Architectural model hardware – software partitioning, distributed system co-synthesis.

UNIT III

PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping, system communication infrastructure

UNIT IV

TARGET ARCHITECTURES: Architecture Specialization techniques, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), and Mixed Systems.

UNIT V

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT VI

DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT VII

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-I: System – level specification, design representation for system level synthesis, system level specification languages,

UNIT VIII

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN-II: Heterogeneous specifications and multi language co-simulation the cosyma system and lycos system.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, "Hardware / software co- design Principles and Practice", Springer, 2009.
2. Kluwer, "Hardware / software co- design Principles and Practice", academic publishers,2002.

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(D0615102) FPGA ARCHITECTURE & APPLICATIONS

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, FPGA – Features, Complex Programmable Logic Devices: ALTERA CPLDs and ALTERA FLEX 10k Series CPLD, Speed Performance.

UNIT II

FPGA: Xilinx logic Cell array, CLB,I/O Block Programmable interconnect, Technology Mapping for FPGA: Library based, LUT based, Multiplexer based Technology Mapping.

UNIT III

CASE STUDIES: programming Technologies, Xilinx XC3000, XC4000, Actel FPGAs, Alteras FPGAs, Plus Logic FPGA, AMD FPGA, Quick Logic FPGA, Algotronix FPGA, Cross point solutions FPGA, FPGA Design Flow.

UNIT IV

FINITE STATE MACHINES (FSM): Finite State Machine– State Transition Table, State Assignments for FPGAs. Problem of the Initial State Assignment for One Hot Encoding.

UNIT V

REALIZATION OF STATE MACHINE: Derivation of SM Charts. Realization of State Machine Chart, Alternative Realization of State Machine Chart using Microprogramming. Linked State Machines. One–Hot State Machine, Petri nets for State Machines – Basic Concepts, Properties. Extended Petri nets for Parallel Controllers.

UNIT VI

FSM ARCHITECTURES: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around A Shift Register.

UNIT VII

SYSTEMS LEVEL DESIGN One–Hot Design Method. Use of ASMs in One–Hot Design. Application of One–Hot Method. System Level Design: Controller, Data Path and Functional Partition.

UNIT VIII

DIGITAL FRONT END DIGITAL DESIGN FOR FPGAS & ASIC: Using Xilinx ISE EDA Tool Guidelines, Case Studies of Parallel Adder Cell, Parallel Adder, Sequential Circuits: Decade Counters, Parallel Multipliers, Parallel Controllers.

TEXT BOOKS/ REFERENCES:

1. Fundamentals of logic Design, 5/e, Charles H Roth.Jr
2. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.
3. S. Brown, R. Francis, J. Rose, Z. Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
4. Engineering Digital Design, 2/e, Richard F Tinder **Unit VI & VII**
5. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.

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(D5509102) CMOS DIGITAL IC DESIGN

UNIT I

MOS Transistor: MOS Structure, MOS System under external bias, Structure and operation of MOSFET, Threshold voltage, MOSFET operation: A qualitative view.

UNIT II

MOSFET Current-voltage characteristics: Gradual channel approximation, Channel length modulation, Substrate bias effect, Constant field scaling, constant voltage scaling, short channel effects, Narrow channel effects.

UNIT III

MOSFET Models and Capacitance: Oxide-related capacitance, Junction capacitance. Level1, Level2, Level 3 modeling equations.

UNIT IV

CMOS Inverter: Circuit operation, calculation of $V_{IL,}$ $V_{IH,}$ $V_{th.}$ Design of CMOS inverters, Supply scaling in CMOS inverter, Power and area considerations.

UNIT V

CMOS Inverter switching characteristics: Delay-time definition, calculation of delay times, Inverter design with delay constraints.

UNIT VI

Estimation of Interconnects parasitic: Interconnect capacitance estimation, Interconnect resistance estimation. Calculation of Interconnect delay: RC delay Models, The Elmore delay, switching power dissipation of CMOS inverter, Power delay product.

UNIT VII

Sequential MOS logic circuits: Behavior of Bi-stable elements, SR Latch circuit, Clocked SR latch, Clocked JK Latch, Master-Slave flip-flop, CMOS D-Latch and Edge-Triggered Flip-Flop.

UNIT VIII

Low Power CMOS logic circuits: Switching power dissipation, Short-circuit power dissipation, Leakage power dissipation, Influence of voltage scaling on Power and delay, Variable-Threshold CMOS (VTCMOS) circuits, Multiple-Threshold CMOS(MTCMOS) circuits, Pipeline approach, Parallel processing approach(Hardware replication).

TEXT BOOKS:

1. Sung-Mo Kang & Yusuf Leblebici, "CMOS Digital Integrated Circuits - Analysis & Design", MGH, Second Ed., 1999
2. Jan M Rabaey, "Digital Integrated Circuits - A Design Perspective", Prentice Hall, 1997.

REFERENCES:

1. Eugene D Fabricus, "Introduction to VLSI Design,"McGraw Hill International Edition.1990.
2. R. J. Baker, H. W. Li, and D. E. Boyce, "CMOS circuit design, layout, and simulation". New York: IEEE Press, 1998.
3. Ken Martin, "Digital Integrated Circuit Design", Oxford University Press, 2000.

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(D0605101) DIGITAL DESIGN THROUGH VERILOG

(ELECTIVE - II)

UNIT I

INTRODUCTION TO VERILOG: Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches.

LANGUAGE CONSTRUCTS AND CONVENTIONS : Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

UNIT II

GATE LEVEL MODELING: Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip-flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits, Exercises.

UNIT III

BEHAVIORAL MODELING: Introduction, Operations and Assignments, Functional Bifurcation, *Initial* Construct, *Always* Construct, Examples, Assignments with Delays, *Wait* construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non blocking Assignments, The *case* statement, Simulation Flow. *if* and *if-else* constructs, *assign-deassign* construct, *repeat* construct, *for* loop, the *disable* construct, *while* loop, *forever* loop, parallel blocks, *force-release* construct, Event.

UNIT IV

MODELING AT DATA FLOW LEVEL: Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators.

SWITCH LEVEL MODELING: Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets, Exercises.

UNIT V

SYSTEM TASKS, FUNCTIONS AND COMPILER DIRECTIVES: Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations, Exercises.

FUNCTIONS, TASKS, AND USER-DEFINED PRIMITIVES: Introduction, Function, Tasks, User-Defined Primitives (UDP), FSM Design (Moore and Mealy Machines).

UNIT VI

DIGITAL DESIGN WITH SM CHARTS: State Machine Charts, Derivation of SM Charts, Realization of SM Charts, Implementation of the Dice Game, Alternative realizations for SM Charts using Microprogramming, Linked State Machines.

UNIT VII

DESIGNING WITH PROGRAMMABLE GATE ARRAYS AND COMPLEX PROGRAMMABLE LOGIC DEVICES: Xilinx 3000 Series FPGAs, Designing with FPGAs, Using a One-Hot State Assignment, Altera Complex Programmable Logic Devices (CPLDs), Altera FLEX 10K Series CPLDs.

UNIT VIII

VERILOG MODELS: Static RAM Memory, A simplified 486 Bus Model, Interfacing Memory to a Microprocessor Bus, UART Design, Design of Microcontroller CPU.

TEXT BOOKS:

1. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, 2004 IEEE Press.
2. A Verilog Primier – J. Bhaskar, BSP, 2003.

REFERENCES:

1. Fundamentals of Logic Design with Verilog – Stephen. Brown and Zvonko Vranesic, TMH, 2005.
2. Digital Systems Design using VHDL – Charles H Roth, Jr. Thomson Publications, 2004.
3. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005.
4. Verilog HDL – 2nd Edition – Samir Palnitkar, Pearson Education.

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(D55101102) LOW POWER VLSI DESIGN

(ELECTIVE - II)

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II

MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration considerations.

UNIT III

Bi-CMOS Isolation considerations.

UNIT IV

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS.

UNIT V

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models,

UNIT VI

Sub-half micron MOS devices: Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT VII

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

UNIT VIII

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

TEXT BOOKS:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl (3 Authors)-Pearson Education Asia 1st Indian reprint,2002.
2. Gary K. Yeap, "Practical Low Power Digital VLSI Design", KAP, 2002.

REFERENCES:

1. Basic VLSI Design, Douglas A.Pucknell & Kamran Eshraghian,3rd edition PHI.
2. Digital Integrated circuits, J.Rabaey PH. N.J 1996
3. CMOS Digital ICs Sung-mo Kang and yusuf leblebici 3rd edition TMH 2003 .
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

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(D0608101) NETWORK SECURITY & CRYPTOGRAPHY

(ELECTIVE - II)

UNIT I

INTRODUCTION: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internet work security. CLASSICAL TECHNIQUES: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT II

MODERN TECHNIQUES: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

ALGORITHMS: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

UNIT III

CONVENTIONAL ENCRYPTION: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

PUBLIC KEY CRYPTOGRAPHY: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT IV

NUMBER THEORY: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

MESSAGE AUTHENTICATION AND HASH FUNCTIONS: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT V

HASH AND MAC ALGORITHMS: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. DIGITAL SIGNATURES AND AUTHENTICATION PROTOCOLS: Digital signatures, Authentication Protocols, Digital signature standards.

UNIT VI

AUTHENTICATION APPLICATIONS: Kerberos, X.509 directory Authentication service. ELECTRONIC MAIL SECURITY: Pretty Good Privacy, S/MIME.

UNIT VII

IP SECURITY: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

WEB SECURITY: Web Security requirements, secure sockets layer and Transport layer security, Secure Electronic Transaction.

UNIT VIII

INTRUDERS, VIRUSES AND WORMS: Intruders, Viruses and Related threats. FIRE WALLS: Fire wall Design Principles, Trusted systems.

TEXT BOOKS

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education., 2000.

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3 **2**

(D5592102) REAL TIME OPERATING SYSTEMS LAB

Testing RTOS Environment and System Programming USING KEIL TOOLS

1. Program for two separate LED blinking tasks.

2. Implement priority scheduling and three different UART transmitting task using OS Delay functions.

3. Multitasking program for
   a) RTC to display LCD 1st line continuously.
   b) ADC to display LCD 2nd line continuously

4. Multitasking, three tasks
   a) Read key input and display on 7 segment display.
   b) Read analog input(ADC) and plot corresponding signal on a GLCD
   c) Generate PWM signal with Xon time and Yoff time.

5. Stepper motor speed control using RTOS delay functions.

6. Real-time operating system kernel (thread switching and synchronization).

7. Blocking semaphores, priority scheduling, performance measures, dumping RTOS profile data to the PC

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3 **2**

(D5593102) CMOS DIGITAL IC DESIGN LAB

Design and Layout generation using **MICROWIND TOOL**

1. Basic Logic Gates.
2. 74x138
3. 74x151
4. 74x157
5. 74x280
6. 74x382
7. 74x74
8. 74x163
9. 74x194
10. Counters- Ring Counter, Johnson Counter, Mod counters
11. Finite State Machine- Mealy and Moore Machines
12. Dual Priority encoder
13. Floating point encoder
14. Error correcting code with hamming code

Analyze the above design with respect to Power consumption, Critical Path delay and Area.