RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY
AUTONOMOUS
ELECTRONICS AND COMMUNICATION ENGINEERING

Affiliated to JNTU-Anantapur, Approved by AICTE-New Delhi, Accredited by NBA-New Delhi

NANDYAL-518 501, KURNOOL Dist., A.P.

DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

ACADEMIC REGULATIONS,
COURSE STRUCTURE AND SYLLABI

APPLICABLE FOR STUDENTS ADMITTED INTO

M.TECH (REGULAR) FROM 2010-11

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REGULATIONS

For pursuing Two year Master (post graduate) Degree of study in Engineering (M.Tech), offered by Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal-518501 under Autonomous status and herein referred to as RGMCET (Autonomous)

All the rules specified herein approved by the Academic Council will be in force and applicable to students admitted from the Academic Year 2010-11 onwards. Any reference to "Institute" or "College" in these rules and regulations stands for Rajeev Gandhi Memorial College of Engineering and Technology (Autonomous).

All the rules and regulations, specified here after shall be read as a whole for the purpose of interpretation as and when a doubt arises , the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, Rajeev Gandhi Memorial College of Engineering and Technology shall be the Chairman, Academic Council.

I. ACADEMIC REGULATIONS 2010 FOR M.TECH (REGULAR)

(Effective for the students admitted into first year from the Academic Year 2010-2011)

THE M.TECH DEGREE OF JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY, ANANTAPUR, SHALL BE CONFERRED ON CANDIDATES WHO ARE ADMITTED TO THE M.TECH PROGRAM AT RGMCET, NANDYAL AND THEY SHALL FULFIL ALL THE REQUIREMENTS FOR THE AWARD OF THE DEGREE.

1.0 Eligibility for Admissions:

Admission to the above program shall be made subject to the eligibility, qualifications and specialization prescribed by Andhra Pradesh State Council of Higher Education (APSCHE) from time to time.

Admissions shall be made on the basis of merit rank obtained in GATE examination or PGCET conducted by any University of Andhra Pradesh designated by Govt. of A.P., or on the basis of any other order of merit prescribed by APSCHE, subject to the reservations prescribed by the Government of A.P. from time to time.

2.0 Award of M.Tech Degree:

2.1) The student shall be declared eligible for the award of the M.Tech degree, if he pursues a course of study and completes it successfully for not less than prescribed course work duration and not more than double the prescribed course work duration.

2.2) The student, who fails to fulfil all the academic requirements for the award of the degree within double the course work duration from the year of his admission, shall forfeit his seat in M.Tech course.

2.2) The minimum clear instruction days for each semester shall be 95.

3.0 Courses of Study:

The following specializations are offered at present for the M.Tech course of study.

1. Computer Science (CSE)
2. Digital Systems and Computer Electronics (ECE)
3. Embedded Systems (ECE)
4. Machine Design (ME)
5. Power Electronics (EEE)
6. Software Engineering (IT)

and any other course as approved by the appropriate authorities from time to time.

4.0 Course pattern:

4.1) The entire course of study is of four semesters. During the first and second semesters the student has to undergo course work and during the third and fourth semesters the student has to carry out project work.

4.2) The student eligible to appear for the End Examination in a subject, but absent at it or has failed in the End Examination may appear for that subject at the supplementary examination.

TABLE 1: CREDITS

	SEMESTER			
	Periods/ Week	Credits	Internal Marks	External Marks
Theory	04	04	40	60
Practical	03	02	40	60
Seminar		02	100	
Comprehensive Viva-voce		04		100
Project		12		

TABLE: 2 COURSE PATTERN

Semester	No.of Subjects	Number of Labs	Total Credits	
First	06	02	6X4=24 2X2=04	28
Second	06	02 Comprehensive Viva	6X4=24 2X2=04 1X4=04	32
Third	Seminar(3^{rd} semester) Project Work			02
Fourth				12
Total credits				74

5.0 Attendance:

5.1) The candidate shall be deemed to have eligibility to write end semester examinations if he has secured a minimum of 75% of attendance in aggregate of all the subjects.

5.2) Condonation of shortage of attendance up to 10% i.e. 65% and above and below 75% may be given by the College academic committee consisting of Principal, Head of the Department and a senior faculty member.

5.3) Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence.

5.4) **Shortage of attendance below 65% shall in no case be condoned**.

5.5) The candidate shall not be promoted to the next semester unless he fulfils the attendance requirements of the previous semester.

6.0 Evaluation:

The performance of the candidate in each semester shall be evaluated subject wise, with a maximum of 100 marks for Theory and 100 marks for practicals, on the basis of Internal Evaluation and End Semester Examination.

6.1) For the theory subjects 60 marks shall be for the External End Examination, While 40 marks shall be for Internal Evaluation, based on the better of the marks secured in the two Mid Term-Examinations held, one in the middle of the Semester (I-IV units) and another immediately After the completion of instruction (V-VIII) units with four questions to be answered out of six, evaluated for 40 marks. Each question carries 10 marks. Each midterm examination shall be

conducted for duration of 120 minutes. The End Examination will have 08 questions and 5 questions are to be answered and each question carries 12 marks.

6.2) For practical subjects, 60 marks shall be for the End Semester Examinations and 40 marks shall be for Internal evaluation based on the day-to-day performance. End practical examinations for M.Tech courses will be conducted with two Examiners, one of them being Laboratory Class Teacher and second Examiner shall be external from other institution.

6.3) Student has to undergo a comprehensive viva pertaining to his specialization which carries 100 marks. He has to secure 50% marks to obtain required credits. Comprehensive viva will be held at the end of II semester with HOD, senior faculty member and external Examiner from outside the institute. For this, HOD of the Department shall submit a panel of 5 Examiners, who are eminent in that field. One from the panel will be selected by the principal of the institute as external Examiner for comprehensive viva.

6.4) For Seminar100 marks shall be for Internal evaluation. The candidate has to secure a minimum of 50 marks to be declared successful. The assessment will be made by a board consisting of HOD and two Internal experts at the end of III semester.

6.5) The candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Examination and Internal evaluation taken together.

6.6) In case the candidate does not secure the minimum academic requirement in any subject(as specified in 6.5.) he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the course when next offered or do any other specified subject as may be required.

7.0 Re-registration for improvement of Internal marks:

Following are the conditions to avail the benefit of improvement of internal marks.

7.1) The candidate should have completed the course work and obtained examinations results for I & II semesters.

7.2) He should have passed all the subjects for which the internal marks secured are more than 50%.

7.3) Out of the subjects the candidate has failed in the examination due to lack of Internal marks secured being less than 50%, the candidate shall be given one chance for Theory subject and subject to a maximum of three Theory subjects.

7.4) The candidate has to re-register for the chosen subjects and fulfil the academic requirements as and when they are offered.

7.5) For each subject, the candidate has to pay a fee equivalent to one third of the semester tuition fee and the amount is to be remitted in the form of D.D. in favour of the Principal, RGMCET payable at RGMCET Nandyal branch along with the requisition through the HOD of the respective Department.

7.6) In case of availing the Improvement of Internal marks, the Internal marks as well as the End Examinations marks secured in the previous attempt(s) for the reregistered subjects stand cancelled.

8.0 Evaluation of Project / Dissertation work :

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Department.

8.1) Registration of Project work: The candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses (theory and practical courses of I & II Sem).

8.2) An Internal Department Committee (I.D.C) consisting of HOD, Supervisor and One Internal senior expert shall monitor the progress of the project work.

8.3) The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

8.4) The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C before submission of the Project Report.

8.5) The candidate shall be allowed to submit the thesis / dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva voce examination of the project. The viva voce examination may be conducted once in two months for all the candidates submitted during that period.

8.6) Three copies of the Thesis / Dissertation certified in the prescribed form by the supervisor & HOD shall be submitted to the institute.

8.7) The Department shall submit a panel of three experts for a maximum of 5 students at a time. However, the thesis / dissertation will be adjudicated by the board consists of HOD, concerned supervisor and one external Examiner from other institute nominated by the principal from a panel of Examiners submitted by the Department to the Controller of Examinations.

8.8) If the report of the board is favourable in viva voce examination, the board shall jointly report candidates work as:

1. Satisfactory
2. Not satisfactory

If the report of the viva voce is not satisfactory the candidate will retake the viva voce examination after three months. If he fails to get a satisfactory report at the second viva voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the thesis.

9.0 Award of Degree and Class:

After the student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following classes:

TABLE 3: AWARD OF DIVISION

Class Awarded	% of marks to be secured	From the aggregate marks secured form the 74 Credits.
First Class with Distinction	70% and above	
First Class	Below 70% but not less than 60%	
Second Class	Below 60% but not less than 50%	

(The marks in Internal evaluation and End Examination shall be shown separately in the marks memorandum)

10.0 Supplementary Examinations:

Apart from the regular End Examinations the institute may also schedule and conduct supplementary examinations for all subjects for the benefit of students with backlogs. Such of the students writing supplementary examinations as supplementary candidates may have to write more than one examination per day.

11.0 Transcripts:

After successful completion of prerequisite credits for the award of degree a Transcript containing performance of all academic years will be issued as a final record. Duplicate transcripts will also be issued if required after the payment of requisite fee and also as per norms in vogue.

12.0 Minimum Instruction Days:

The minimum instruction days for each semester shall be 95 clear instruction days excluding the days allotted for tests/examinations and preparation holidays declared if any.

13.0 Amendment of Regulations:

The college may, from time to time, revise, amend or change the regulations, scheme of examinations and syllabi. However the academic regulations of any student will be same throughout the course of study in which the student has been admitted.

14.0 Transfers

There shall be no branch transfers after the completion of admission process.

15.0 With holding of results:

If the candidate has not paid any dues to the institute or if any case of in-discipline is pending against him, the result of the candidate will be with held and he will not be allowed for the next semester. The issue of the degree is liable to be withheld in such cases.

16.0 Transitory Regulations:

Candidates who have discontinued or have been detained for want of attendance are eligible for admission to the same or equivalent subjects as and when subjects are offered, subject to 6.5 and 2.0

17.0 Rules of Discipline:

17.1) Any attempt by any student to influence the teachers, Examiners, faculty and staff of controller of Examination for undue favours in the exams, and bribing them either for marks or

attendance will be treated as malpractice cases and the student can be debarred from the college.

17.2) When The student absents himself, he is treated as to have appeared and obtained zero marks in that subject(s) and grading is done accordingly.

17.3) When the performance of the student in any subject(s) is cancelled as a punishment for indiscipline, he is awarded zero marks in that subject(s).

17.4) When the student's answer book is confiscated for any kind of attempted or suspected malpractice the decision of the Examiner is final.

18.0 General:

18.1) The Academic Regulation should be read as a whole for the purpose of any interpretation.

18.2) In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the College Academic Council is final.

18.3) The Institute may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Institute.

18.4) Where the words "he", "him", "his", occur in the regulations, they include "she", "her", "hers".

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

COURSE STRUCTURE

I M.TECH, I-SEMESTER

Code	Subject	Scheme of instruction periods/week		Credits	Scheme of Examination		
		Theory	Practical		Internal	External	Total
D0601101	Digital System Design	4		4	40	60	100
D0602101	Embedded System Concepts	4		4	40	60	100
D0603101	Advanced Computer Architecture	4		4	40	60	100
D0604101	Advanced Data Communications	4		4	40	60	100
D0605101	Digital Design through Verilog	4		4	40	60	100
	ELECTIVE-I	4		4	40	60	100
D0606101	DSP Processors and Architectures						
D0607101	Experts systems						
D0608101	Network Security & Cryptography						
D0691101	FPGA/CPLD Lab		3	2	40	60	100
D0692101	Embedded System Lab		3	2	40	60	100
	Total	**24**	**6**	**28**	**320**	**480**	**800**

I M.TECH, II-SEMESTER

Code	Subject	Scheme of instruction periods/week		Credits	Scheme of Examination		
		Theory	Practical		Internal	External	Total
D0609102	Micro Computer Systems Design	4		4	40	60	100
D0610102	Neural Networks & Applications	4		4	40	60	100
D0611102	Design of Fault Tolerant Systems	4		4	40	60	100
D0612102	Systems Programming	4		4	40	60	100
D0613102	Image & Video Processing	4		4	40	60	100
	ELECTIVE-II	4		4	40	60	100
D0614102	System Modeling and Simulation.						
D5505101	Algorithms for VLSI Design Automation						
D0615102	FPGA Architecture & Applications						
	LABORATORY						
D0693102	Signal Processing & Micro Processors Lab		3	2	40	60	100
D0694102	Neural Networks using MATLAB		3	2	40	60	100
D0695102	Comprehensive Viva			4		100	100
	Total	**24**	**6**	**32**	**320**	**580**	**900**

II M.TECH, III-SEMESTER & IV-SEMESTER

Code	**Subject**	**Credits**	**Internal Marks**	**External Marks**	**Total**
D0696103	Seminar (End of III Semester)	2	100	-	100
D0697104	Project work	12	-	-	-

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech I-Sem (DSCE) **T C**

4 4

(D0601101) DIGITAL SYSTEM DESIGN

UNIT I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

UNIT II

SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT III

FAULT MODELING: Fault classes and models, stuck at faults, bridging faults, transition and intermittent faults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT IV

TEST PATTERN GENERATION: D–algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT V

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT VI

PROGRAMMING LOGIC ARRAYS: Design using PLA's, PLA minimization and PLA folding.

UNIT VII

PLA TESTING: Fault models, Test generation and Testable PLA design.

UNIT VIII

ASYNCHRONOUS SEQUENTIAL MACHINE: Fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXTBOOKS:

1. Kohavi – "Switching & finite Automata Theory" (TMH)
2. N. Biswas – "Logic Design Theory" (PHI)
3. olman Balabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition 2004.

REFRENCES:

1. M.Abramovici, M.A.Breues, A.D. Friedman – "Digital System Testing and Testable Design", Jaico Publications
2. Charles H. Roth Jr. – "Fundamentals of Logic Design".
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4th Edition

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech I-Sem (DSCE) **T C**

4 4

(D0602101) EMBEDDED SYSTEM CONCEPTS

Unit I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems

Unit II

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

Unit III

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space

Unit IV

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

Unit V

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes

Unit VI

INSTRUCTION SETS: Introduction, preliminaries, ARM processor, SHARC processor.

Unit VII

SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications, system analysis and architecture design

Unit VIII

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes , etc

TEXT BOOKS:

1) Computers as a component: principles of embedded computing system design- wayne wolf
2) An embedded software premier: David E. Simon
3) Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1) Embedded real time systems programming-sri ram V Iyer, pankaj gupta, TMH, 2004.
2) Embedded system design- A unified hardware/software introduction- frank vahid, tony D. Givargis, John Willey, 2002.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech I-Sem (DSCE) **T C**

4 4

(D0603101) ADVANCED COMPUTER ARCHITECTURE

UNIT I

FUNDAMENTALS OF COMPUTER DESIGN: Technology trends, cost- measuring and reporting performance quantitative principles of computer design.

UNIT II

INSTRUCTION SET PRINCIPLES AND EXAMPLES: classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set-instructions for control flow- encoding an instruction set.-the role of compiler

UNIT III

INSTRUCTION LEVEL PARALLELISM (ILP): over coming data hazards, reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP

UNIT IV

ILP SOFTWARE APPROACH: Compiler Techniques, Static Branch Protection, VLIW Approach, H.W support for more ILP at compile time- H.W verses S.W solutions

UNIT V

MEMORY HIERARCHY DESIGN: cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

UNIT VI

MULTIPROCESSORS AND THREAD LEVEL PARALLELISM: symmetric shared memory architectures, distributed shared memory, Synchronization, multi threading.

UNIT VII

STORAGE SYSTEMS: Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

UNIT VIII

INTER CONNECTION NETWORKS AND CLUSTERS: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster

TEXT BOOKS:

1. John. Hennessy & David A. Patterson Morgan Kufmann, "Computer Architecture A quantitative approach", 3rd edition (An Imprint of Elsevier)

REFERENCES:

1. Kai Hwang and A. Briggs, "Computer Architecture and parallel Processing", International Edition McGraw-Hill.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, "Advanced Computer Architectures", Pearson.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech I-Sem (DSCE) **T C**

4 4

(D0604101) ADVANCED DATA COMMUNICATIONS

UNIT I

DIGITAL MODULATION: Introduction, Information Capacity Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK, Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

UNIT II

BASIC CONCEPTS OF DATA COMMUNICATIONS, INTERFACES AND MODEMS: Data Communication, Components, Networks, Distributed Processing, Network Criteria- Applications, Protocols and Standards, Standards Organizations, Regulatory Agencies.

UNIT III

Line Configuration- Point-to-point- Multipoint, Topology, Mesh, Star, Tree, Bus, Ring, Hybrid Topologies, Transmission Modes, Simplex, Half duplex- Full Duplex, Categories of Networks- LAN, MAN, WAN and Internetworking, Digital Data Transmission- Parallel and Serial, DTE-DCE Interface-Data Terminal Equipment, Data Circuit-Terminating Equipment, Standards EIA 232 Interface, Other Interface Standards, Modems- Transmission Rates.

UNIT IV

ERROR DETECTION AND CORRECTION: Types of Errors- Single- Bit Error, CRC (Cyclic Redundancy Check), Performance, Checksum, Error Correction- Single-Bit Error Correction, Hamming Code.

UNIT V

DATA LINK CONTROL: Stop and Wait, Sliding Window Protocols.

DATA LINK PROTOCOLS: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocol- Binary Synchronous Communication (BSC) - BSC Frames- Data Transparency, Bit Oriented Protocols, HDLC, Link Access Protocols.

UNIT VI

SWITCHING*:* Circuit Switching- Space Division Switches- Time Division Switches, TDM Bus, Space and Time Division Switching Combinations, Public Switched Telephone Network, Packet Switching- Datagram Approach- Virtual Circuit Approach, Circuit Switched Connection Versus Virtual Circuit Connection, Message Switching.

MULTIPLEXING: Time Division Multiplexing (TDM), Synchronous Time Division Multiplexing, Digital Hierarchy, Statistical Time Division Multiplexing.

UNIT VII

MULTIPLE ACCESS: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Detection (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization-

UNIT VIII

Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), - Code - Division Multiple Access (CDMA).

TEXT BOOKS:

1) B. A.Forouzan, "Data Communication and Computer Networking", 3rd ed., TMH, 2008.
2) W. Tomasi, "Advanced Electronic Communication Systems", 5 ed., PEI2008.

REFERENCES:

1) Prakash C. Gupta, "Data Communications and Computer Networks", PHI, 2006.
2) William Stallings, "Data and Computer Communications", 8th ed., PHI 2007.
3) T. Housely, "Data Communication and Tele Processing Systems", 2nd Edition, BSP, 2008.
4) Brijendra Singh, "Data Communications and Computer Networks", 2nd ed., PHI 2005.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech I-Sem (DSCE) **T C**

4 4

(D0605101) DIGITAL DESIGN THROUGH VERILOG

UNIT I

INTRODUCTION TO VERILOG : Verilog as HDL, Levels of Design Description, Concurrency, Simulation and Synthesis, Functional Verification, System Tasks, Programming Language Interface (PLI), Module, Simulation and Synthesis Tools, Test Benches.

LANGUAGE CONSTRUCTS AND CONVENTIONS : Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

UNIT II

GATE LEVEL MODELING : Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip-flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits, Exercises.

UNIT III

BEHAVIORAL MODELING : Introduction, Operations and Assignments, Functional Bifurcation, *Initial* Construct, *Always* Construct, Examples, Assignments with Delays, *Wait* construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non blocking Assignments, The *case* statement, Simulation Flow. *if* and *if-else* constructs, *assign-deassign* construct, *repeat* construct, *for* loop, the *disable* construct, *while* loop, *forever* loop, parallel blocks, *force-release* construct, Event.

UNIT IV

MODELING AT DATA FLOW LEVEL : Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators.

SWITCH LEVEL MODELING.

Introduction, Basic Transistor Switches, CMOS Switch, Bi-directional Gates, Time Delays with Switch Primitives, Instantiations with Strengths and Delays, Strength Contention with Trireg Nets, Exercises.

UNIT V

SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES : Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations, Exercises,

FUNCTIONS, TASKS, AND USER-DEFINED PRIMITIVES : Introduction, Function, Tasks, User-Defined Primitives (UDP), FSM Design (Moore and Mealy Machines)

UNIT VI

DIGITAL DESIGN WITH SM CHARTS : State Machine Charts, Derivation of SM Charts, Realization of SM Charts, Implementation of the Dice Game, Alternative realizations for SM Charts using Microprogramming, Linked State Machines.

UNIT VII

DESIGNING WITH PROGRAMMABLE GATE ARRAYS AND COMPLEX PROGRAMMABLE

LOGIC DEVICES : Xilinx 3000 Series FPGAs, Designing with FPGAs, Using a One-Hot State Assignment, Altera Complex Programmable Logic Devices (CPLDs), Altera FLEX 10K Series CPLDs.

UNIT VIII

VERILOG MODELS: Static RAM Memory, A simplified 486 Bus Model, Interfacing Memory to a Microprocessor Bus, UART Design, Design of Microcontroller CPU.

TEST BOOKS:

1. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, 2004 IEEE Press.
2. A Verilog Primier – J. Bhaskar, BSP, 2003.

REFERENCES:

1. Fundamentals of Logic Design with Verilog – Stephen. Brown and Zvonko Vranesic, TMH, 2005.
2. Digital Systems Design using VHDL – Charles H Roth, Jr. Thomson Publications, 2004.
3. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005.
4. Verilog HDL – 2nd Edition – Samir Palnitkar, Pearson Education.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech I-Sem (DSCE) **T C**

4 4

(D0606101) DSP PROCESSORS AND ARCHITECTURES

(ELECTIVE - I)

UNIT I

INTORODUCTION TO DIGITAL SIGNAL PROCESING: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS : Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT IV

EXECUTION CONTROL AND PIPELINING: Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT V

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX processors, Pipeline Operation of TMS320C54XX Processors.

UNIT VI

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT VII

IMPLEMENTATION OF FFT ALGORITHMS: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT VIII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES:

Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS :

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features – Lapsley et al. S. Chand & Co, 2000.

REFERENCES :

1. Digital Signal Processors, Architecture, Programming and Applications – B. Venkata Ramani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

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M.Tech I-Sem (DSCE) **T C**

4 4

(D0607101) EXPERT SYSTEMS

(ELECTIVE - I)

UNIT I

KNOWLEDGE REPRESENTATION AND ISSUES: Notational systems: Trees, graphs, hierarchies, propositional and predicate logics, frames, semantics networks, constraints, conceptual dependencies, database, knowledge discovery in databases (KDD).

UNIT II

SEARCH: State-space representations, Depth-first, breadth-first, heuristic search, Planning and game playing, Genetic algorithms.

UNIT III

LOGICAL REASONING AND PROBABILISTIC REASONING: Predicate, Calculus resolution, completeness, and strategies, Unification, Prolog, monotonic and non-monotonic reasoning.

UNIT IV

Probabilistic inference networks, Fuzzy inference rules, Bayesian rules. Dempster-Shafer Calculus.

UNIT V

LEARNING AND COMMON SENSANE REASONING: Robot actions, strips, triangle tables, case based reasoning, spatial and temporal formalisms.

UNIT VI

Knowledge acquisition, classification rules, self directed systems.

UNIT VII

NEURAL NETWORKS: Principles, biological analogies, Training (techniques and errors), Recognition.

UNIT VIII

EXPERT SYSTEMS Expert Systems, Organization, tools, limits, examples.

TEXT BOOKS:

1. Charniak .E,And McDermott .D., ”Intoduction to Artificial intelligence”, Adiison-Wesley, 1987
2. Giarratano.J.,And Riley G., ”Expert Systems principles an Programming” PWS-KENT,1989

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M.Tech I-Sem (DSCE) **T C**

4 4

(D0608101) NETWORK SECURITY & CRYPTOGRAPHY

(ELECTIVE - I)

UNIT I

INTRODUCTION: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internet work security. CLASSICAL TECHNIQUES: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT II

MODERN TECHNIQUES: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.
ALGORITHMS: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

UNIT III

CONVENTIONAL ENCRYPTION: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.
PUBLIC KEY CRYPTOGRAPHY: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT IV

NUMBER THEORY: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.
MESSAGE AUTHENTICATION AND HASH FUNCTIONS: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT V

HASH AND MAC ALGORITHMS: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC. DIGITAL SIGNATURES AND AUTHENTICATION PROTOCOLS: Digital signatures, Authentication Protocols, Digital signature standards.

UNIT VI

AUTHENTICATION APPLICATIONS: Kerberos, X.509 directory Authentication service. ELECTRONIC MAIL SECURITY: Pretty Good Privacy, S/MIME.

UNIT VII

IP SECURITY: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.
WEB SECURITY: Web Security requirements, secure sockets layer and Transport layer security, Secure Electronic Transaction.

UNIT VIII

INTRUDERS, VIRUSES AND WORMS: Intruders, Viruses and Related threats. FIRE WALLS: Fire wall Design Principles, Trusted systems.

TEXT BOOKS

1.Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education., 2000.

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M.Tech I-Sem (DSCE) **P C**

3 2

(D0691101) FPGA/CPLD LAB

1. Simulation and Verification of Logic Gates.
2. Simulation and Verification of 74x138
3. Simulation and Verification of 74x151
4. Simulation and Verification of 74x157
5. Simulation and Verification of 74x280
6. Simulation and Verification of 74x382
7. Simulation and Verification of 74x74
8. Simulation and Verification of 74x163
9. Simulation and Verification of 74x194
10. Design, Simulation of Counters- Ring Counter, Johnson Counter, Mod counters
11. Finite State Machine- Mealy and Moore Machines
12. Design, Simulation and verification of Dual Priority encoder
13. Design, Simulation and verification of Floating point encoder
14. Design, Simulation and verification of Error correcting code with hamming code

Implementation of all the Design using FPGA and CPLD Devices.

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M.Tech I-Sem (DSCE) **P C**

3 2

(D0692101) EMBEDDED SYSTEMS LAB

ASSEMBLY:

1. Write a program to
   a) Clear the Register and
   b) Add 3 to Register Ten Times and Place the Result into Memory Use the Indirect Instructions to Perform Looping.

PROGRAMING IN C:

2. Write a Program to Toggle all the Bits of PORT B parts continuously with a 250ns Delay.

3. Stepper Motor Control using Microcontroller.

4. Use Microcontrollers for the following Experiments.
   a. Elevator Interface.
   b. Key Board Interface.
   c. LED Interface.
   d. Temperature Sensor.
   e. SORT RTO'S on to 89c51 Board.
   f. Sample the Signal using ADC and Reconstruct by using DAC.

5. RTOS System solution & tools

6. Testing RTOS Environment and System Programming (Keil Tools)

7. Embedded DSP based System Designing.
   a) Code compressor studio (CCS) for embedded DSP using Texas tool kit.
   b) Analog DSP tool kit.

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M.Tech II-Sem (DSCE) **T C**

4 4

(D0609102) MICRO COMPUTER SYSTEM DESIGN

UNIT I

REVIEW OF 8086 PROCESSOR: Architecture, Register organization, Addressing Modes and Instruction Set (Brief treatment only), Difference between 8086 and 8088 with rest to pin structures.

UNIT II

THE 80286 MICRO PROCESSORS: Architecture, Register Organization, Addressing Modes and instruction sets of 80286 (brief treatment only)

UNIT III

THE 80386, AND 80486 MICRO PROCESSORS: Architectural features, Register Organization, Memory management, Virtual 8086 mode, The Memory Paging Mechanism, Pin Definitions of 80386 and 80486 (brief treatment).

UNIT IV

THE PENTIUM AND PENTIUM PRO PROCESSORS: The Memory System, Input/output system, Branch Prediction Logic, Cache Structure, Pentium Registers, Serial Pentium pro features.

UNIT V

THE PENTIUM IV AND DUAL CORE MICRO PROCESSORS: Architecture, Special Registers and Pin Structures (brief treatment only)

UNIT VI

I/O PROGRAMMING: Fundamentals of I/O, Considerations Programmed I/O, Interrupt I/O, Block Transfers and DMA, I/O Design Example.

UNIT VII

INTRODUCTION TO MULTIPROGRAMMING: Process Management, Semaphores Operations, Common Procedure Sharing, Memory Management, Virtual Memory Concept of 80286 and other advanced Processors.

UNIT VIII

ARITHMETIC COPROCESSOR, MMX AND SIMD TECHNOLOGIES: Data formals for Arithmetic Coprocessor, Internal Structure of 8087 and Advanced Coprocessors. Instruction Set (brief treatment).

TEXTBOOKS:

1) Barry, B. Brey, "The Intel Microprocessors,"8th Edition Pearson Education, 2009.
2) A.K. Ray and K.M. Bhurchandi, "Advanced Microprocessor and Peripherals" TMH.

REFERENCES:

1. YU-Chang, Glenn A. Gibson, "Micro Computer Systems: The 8086/8088 Family Architecture,
2. Programming and Design" 2nd Edition, Pearson Education, 2007
3. Douglas V. Hall, "Microprocessors and Interfacing," Special Indian Edition, 2006.

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M.Tech II-Sem (DSCE) **T C**
4 4

(D0610102) NEURAL NETWORKS & APPLICATIONS

UNIT I

FUNDAMENTAL CONCEPTS AND MODELS OF ARTIFICIAL NEURAL SYSTEMS: Structure and functions of Biological Neuron, McCulloch-Pitts Neuron Model, Neuron Modeling for Artificial Neural Systems, Models of Artificial Neural Networks: Feed forward Network and feed backward Network. Neural Processing, learning: Supervised and Unsupervised learning

UNIT II

NEURAL NETWORK LEARNING RULES: Hebbian Learning Rule, Perceptron Learning Rule, Delta Learning Rule, Widrow-Hoff learning Rule, Correlation Learning Rule, Winner–Take-All Learning rule, OutStar Learning Rule, summary of Learning rules.

UNIT III

SINGLE- LAYER PERCEPTRON CLASSIFIERS: Classification Model, Features, and Decision Regions, Discriminant Functions, linear Machine and Minimum Distance Classification, Nonparametric training concept, Training and classification using the discrete perceptron, Single Layer Continuous Perceptron Networks for Linearly Separable Classifications. Multicategory Single Layer Perceptron Networks.

UNIT IV

MULTILAYER FEED FORWARD NETWORKS: Linearly nonseparable pattern classification, Delta Learning rule for Multiperceptron layer. Generalized Delta Learning rule. Feed forward Recall and Error Back Propagation Training: Feedforward Recall, Error Back-Propagation Training. Application of Back propagation Networks in pattern recognition & Image processing, Madalines: Architecture & Algorithms.

UNIT V

SINGLE-LAYER FEEDBACK NETWORKS: Basic concepts of Dynamical systems. Mathematical Foundation of Discrete-Time Hop field Networks. Mathematical Foundation of Gradient-Type Hopfield Networks. Transient response of Continuous time Networks. Minimization of the Traveling salesman tour length, Solving Simultaneous Linear Equations.

UNIT VI

ASSOCIATIVE MEMORIES-I: Basic concepts, linear associator, Basic concepts of Recurrent Auto associative memory: Retrieval algorithm. Storage algorithm, Performance considerations.

UNIT VII

ASSOCIATIVE MEMORIES-II: Boltzmann machines, Bidirectional Associative Memory, Associative Memory of Spatio-temporal Patterns

UNIT VIII

MATCHING AND SELF-ORGANIZING NETWORKS: Hamming net and MAXNET, Unsupervised learning of clusters. Clustering and similarity measures, Winner-Take-All learning, Recall mode, initialization of weights, reparability limitations. Counter propagation networks. Feature mapping, Self organizing feature maps, LVPS, Cluster discovery networks (ART1).

TEXT BOOKS

1. J.M.Zurada: Introduction to Artificial Neural Systems, Jaico Publishers
2. Dr. B. Yagananarayana, Artificial Neural Networks, PHI, New Delhi.

REFERENCES

1. Kishan Mehrotra, Chelkuri K. Mohan, Sanjay Ranka: Elements of Artificial Neural Networks, Penram International
2. Artificial Neural Network – By Simon Haykin, Pearson Education
3. Introduction Neural Networks Using MATLAB 6.0 - by S.N. Sivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi.
4. Fundamental of Neural Networks – By Laurene Fausett

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M.Tech II-Sem (DSCE) **T C**

4 4

(D0611102) DESIGN OF FAULT TOLERANT SYSTEMS

UNIT I

BASIC CONCEPTS: Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and Mean time between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.

UNIT II

FAULT TOLERANT DESIGN: Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self purging redundancy, Sift out redundancy (SMR), SMR Configuration, Use of error correcting code, Time redundancy and software redundancy.

UNIT III

SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

UNIT IV

FAIL SAFE DESIGN: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, Totally self checking PLA design.

UNIT V

DESIGN FOR TESTABILITY FOR COMBINATIONAL CIRCUITS: Basic concepts of testability, controllability and observability, the Reed Muller's expansion technique, OR-AND-OR design, use of control and syndrome testable design.

UNIT VI

Theory and operation of LFSR, LFSR as Signature analyzer, Multiple-input Signature Register.

UNIT VII

DESIGN FOR TESTABILITY FOR SEQUENTIAL CIRCUITS: Controllability and observability by means of scan register, Storage cells for scan design, classic scan design, Level Sensitive Scan Design (LSSD).

UNIT VIII

BUILT IN SELF TEST: BIST concepts, Test pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture.

TEXT BOOKS:

1. Parag K. Lala – "Fault Tolerant & Fault Testable Hardware Design" (PHI)
2. M. Abramovili, M.A. Breues, A. D. Friedman – "Digital Systems Testing and Testable Design" Jaico publications.

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M.Tech II-Sem (DSCE) **T C**

4 4

(D0612102) SYSTEMS PROGRAMMING

UNIT I

LANGUAGE PROCESSORS: Introduction, Language Processing Activities, Fundamentals of Language Processing, Fundamental of Language Specifications, Language Processors Development Tools.

UNIT II

DATA STRUCTURES FOR LANGUAGE PROCESSING: Search Data Structures, Allocation Data Structures.

UNIT III

SCANNING ANG PARSING:

Scanning: Introduction, Finite State Automata, regular Expressions, Building DFA's, Performing Semantic Actions, Writing a Scanner.

Parsing: Introduction, Parse Trees and Abstract Syntax Trees, Top Down Parsing and its Algorithm, Predictions and Backtracking, Implementing Top Down Parsing, Comments on Top Down Parsing, Top Down Parsing Without Back Tracking, Practical Top Down Parsing, Bottom Up Parsing and its Algorithm, Simple Precedence, Simple Precedence grammar, Operator Precedence Grammars, Operator Precedence Parsing, Algorithms, LALR Parsing.

UNIT IV

ASSEMBLERS: Elements of Assembly Language Programming, A Simple Assembly Scheme, Pass Structure of Assemblers, A single Pass Assembler for IBM PC.

UNIT V

MACROS AND MACRO PROCESSORS: Macro Definition and Call, Macro Expansion, Nested Macro Calls, Advanced Macro Facilities, Design of Macro Processors.

UNIT VI

COMPILERS AND INTERPRETERS: Aspects of Compilation, Memory Allocation, Compilation of Expressions, Compilation of Control Structures, Code Optimization, Interpreters.

UNIT VII

LINKERS: Relocation and Linking Concepts, Design of Linkers, Self Relocation Programs, A Linker for MS DOS, Linking for Overlays, Loaders.

UNIT VIII

SOFTWARE TOOLS: Software Tools for Program Development, Editors, Debug Monitors, Programming Environments, User Interfaces.

TEXT BOOKS:

1. Systems Programming and Operating Systems by D.M.Dhamdhere, 2nd edition, TMH.

REFERENCES:

1. Systems Programming by John J. Donovan, Mc. Graw Hill International Editions.

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ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech II-Sem (DSCE)

T	C
4	4

(D0613102) IMAGE & VIDEO PROCESSING

UNIT I

IMAGE REPRESENTATION: Gray scale and colour Images, image sampling and quantization. Two dimensional orthogonal transforms: DFT, WHT, Haar transform, KLT, DCT.

UNIT II

IMAGE ENHANCEMENT: Filters in spatial and frequency domains, histogram-based processing, homomorphic filtering. Edge detection, non parametric and model based approaches, LOG filters, localization problem.

UNIT III

IMAGE RESTORATION: Degradation Models, PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods.

UNIT IV

IMAGE SEGMENTATION: Pixel classification, Bi-level Thresholding, Multi-level Thresholding, P-tile method, Adaptive Thresholding, Spectral & spatial classification, Edge detection, Hough transform, Region growing.

UNIT V

FUNDAMENTAL CONCEPTS OF IMAGE COMPRESSION: Compression models, Information theoretic perspective, Fundamental coding theorem.

UNIT VI

LOSSLESS COMPRESSION: Huffman Coding, Arithmetic coding, Bit plane coding, Run length coding, Lossy compression: Transform coding, Image compression standards.

UNIT VII

VIDEO PROCESSING: Representation of Digital Video, Spatio-temporal sampling, Motion Estimation.

UNIT VIII

Video Filtering, Video Compression, Video coding standards.

TEXT BOOKS/REFERENCES:

1. R. C. Gonzalez, R. E. Woods, "Digital Image Processing", Pearson Education. 2nd edition, 2002
2. W. K. Pratt, "Digital image processing", Prentice Hall, 1989
3. A. Rosenfold and A. C. Kak, "Digital image processing", Vols. 1 and 2, Prentice Hall, 1986.
4. H. C. Andrew and B. R. Hunt, "Digital image restoration", Prentice Hall, 1977
5. R. Jain, R. Kasturi and B.G. Schunck, "Machine Vision", McGraw-Hill International Edition, 1995
6. A. M. Tekalp, "Digital Video Processing", Prentice-Hall, 1995
7. Yao Wang, Jorm Ostermann and Ya Qin Zhang "Video Processing and Communications" PHI, 2002.
8. A. Bovik, "Handbook of Image & Video Processing", Academic Press, 2000

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M.Tech II-Sem (DSCE) **T C**

4 4

(D0614102) SYSTEM MODELING & SIMULATION

(ELECTIVE-II)

UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT II

SIMULATION SOFTWARE: Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT III

BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

UNIT IV

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.

UNIT V

EXOGENOUS SIGNALS AND EVENTS: Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation.

UNIT VI

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous-Time Markov processes.

UNIT VII

EVENT DRIVEN MODELS: Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple servers.

UNIT VIII

SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation mythology.

TEXTBOOKS

1. System Modeling & Simulation, An Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFRENCE BOOKS

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

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M.Tech II-Sem (DSCE) **T C**

4 4

(D5505101) ALGORITHMS FOR VLSI DESIGN AUTOMATION

(ELECTIVE II)

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

UNIT IV

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT V

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

UNIT VI

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT VII

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT VIII

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", Wiley Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation", 3rd edition, Springer International Edition, 2005.

REFERENCES:

1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", Wiley, 1993.
2. Wayne Wolf, "Modern VLSI Design: Systems on silicon", Pearson Education Asia, 2nd Edition, 1998.

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ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech II-Sem (DSCE) **T C**

4 4

(D0615102) FPGA ARCHITECTURE & APPLICATIONS

(ELECTIVE II)

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, FPGA – Features, Complex Programmable Logic Devices: ALTERA CPLDs and ALTERA FLEX 10k Series CPLD, Speed Performance.

UNIT II

FPGA: Xilinx logic Cell array, CLB,I/O Block Programmable interconnect, Technology Mapping for FPGA: Library based, LUT based, Multiplexer based Technology Mapping.

UNIT III

CASE STUDIES: programming Technologies, Xilinx XC3000, XC4000, Actel FPGAs, Alteras FPGAs, Plus Logic FPGA, AMD FPGA, Quick Logic FPGA, Algotronix FPGA, Cross point solutions FPGA, FPGA Design Flow.

UNIT IV

FINITE STATE MACHINES (FSM): Finite State Machine– State Transition Table, State Assignments for FPGAs. Problem of the Initial State Assignment for One Hot Encoding.

UNIT V

REALIZATION OF STATE MACHINE: Derivation of SM Charts. Realization of State Machine Chart, Alternative Realization of State Machine Chart using Microprogramming. Linked State Machines. One–Hot State Machine, Petri nets for State Machines – Basic Concepts, Properties. Extended Petri nets for Parallel Controllers.

UNIT VI

FSM ARCHITECTURES: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around A Shift Register.

UNIT VII

SYSTEMS LEVEL DESIGN: One–Hot Design Method. Use of ASMs in One–Hot Design. Application of One–Hot Method. System Level Design: Controller, Data Path and Functional Partition.

UNIT VIII

DIGITAL FRONT END DIGITAL DESIGN FOR FPGAS & ASIC: Using Xilinx ISE EDA Tool Guidelines, Case Studies of Parallel Adder Cell, Parallel Adder, Sequential Circuits: Decade Counters, Parallel Multipliers, Parallel Controllers.

TEXT BOOKS/ REFERENCES:

1) Fundamentals of logic Design, 5/e, Charles H Roth,Jr
2) P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, jPrentice Hall (Pte), 1994.
3) S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
4) Engineering Digital Design, 2/e, Richard F Tinder **Unit VI & VII**
5) J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.

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M.Tech II-Sem (DSCE) **P C**

3 2

(D0693102) SIGNAL PROCESSING & MICROPROCESSORS LAB

1. Design and Simulation FIR Filter Using any Windowing Technique.
2. Design of IIR Filters from Analog Filters.
3. Cancellation of Channel Effects using Adaptive Filter (using LMS / RLS Algorithms).
4 Multirate signal processing.
5. Interface a Seven Segment LED to a Decimal Data source refer Digital System Design and Microprocessor by Hayes Tata McGraw Hill.
6. Interface A/D and D/A, and reconstruct the sampled Signal.
7. Use Interrupt and Sample the Sinusoidal.
8. Interface keyboard and write a Routine to Read a Key from the Keyboard.

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ELECTRONICS AND COMMUNICATION ENGINEERING

M.Tech II-Sem (DSCE) **P** **C**

3 **2**

(D0694102) NEURAL NETWORKS USING MATLAB

1. Realization of Adaline Network
2. Realization of Art Network
3. Realization of Backpropagation Neural Network
4. Realization of Kohonen Network
5. Realization of LVQ Network