RAJEEV GANDHI MEMORIAL

COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

Affiliated to JNTUA -Anantapuramu, Approved by AICTE-New Delhi,
Accredited by NBA-New Delhi, Accredited by NAAC of UGC with A-Grade

NANDYAL-518 501, KURNOOL Dist., A.P.

DEPARTMENT OF

ELECTRONICS AND COMMUNICATION ENGINEERING

DIGITAL SYSTEMS & COMPUTER ELECTRONICS

ACADEMIC REGULATIONS, COURSE STRUCTURE AND SYLLABI

APPLICABLE FOR STUDENTS ADMITTED INTO

M.TECH (REGULAR) FROM 2015-16

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

(Affiliated to J.N.T.U.A, Ananthapuramu)

ACADEMIC REGULATIONS, COURSE STRUCTURE AND DETAILED SYLLABI

M.Tech. (Regular) from 2015-16

For pursuing Two year Master (post graduate) Degree of study in Engineering (M.Tech.), offered by Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal - 518501 under Autonomous status and herein referred to as RGMCET (Autonomous).

All the rules specified herein approved by the Academic Council will be in force and applicable to students admitted from the Academic Year 2015-16 onwards. Any reference to "Institute" or "College" in these rules and regulations shall stand for Rajeev Gandhi Memorial College of Engineering and Technology (Autonomous).

All the rules and regulations, specified hereafter shall be read as a whole for the purpose of interpretation as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, Rajeev Gandhi Memorial College of Engineering and Technology shall be the Chairman, Academic Council.

Academic Regulations 2015 for M.Tech. (Regular)

(Effective for the students admitted into first year from the Academic Year 2015-2016)

The M.Tech. Degree of Jawaharlal Nehru Technological University Anantapur, Ananthapuramushall be conferred on candidates who are admitted to the M.Tech. program at RGMCET, Nandyal and they shall fulfil all the requirements for the award of the Degree.

1.0 Eligibility for Admissions:

Admission to the above program shall be made subject to the eligibility, qualifications and specialization prescribed by Andhra Pradesh State Council of Higher Education (APSCHE) from time to time.

Admissions shall be made on the basis of merit rank obtained in GATE examination or PGCET conducted by any University of Andhra Pradesh designated by Govt. of A. P., or on the basis of any other order of merit prescribed by APSCHE, subject to the reservations prescribed by the Government of A. P. from time to time.

2.0 Award of M.Tech. Degree:

2.1 The student shall be declared eligible for the award of the M.Tech. degree, if he/she pursues a course of study and completes it successfully for not less than prescribed course work duration and not more than double the prescribed course work duration.

2.2 The student, who fails to fulfil all the academic requirements for the award of the degree within double the course work duration from the year of his admission, shall forfeit his seat in M.Tech. course.

2.3 The minimum clear instruction days for each semester shall be 95.

3.0 Courses of Study:

The following specializations are offered at present for the M.Tech. course of study.

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1. Computer Science (CSE)
2. Digital Systems and Computer Electronics (ECE)
3. Embedded Systems (ECE)
4. Machine Design (Mechanical Engineering)
5. Power Electronics (EEE)
6. Software Engineering (IT)
7. Structural Engineering (CE)

and any other course as approved by the appropriate authorities from time to time.

4.0 Course pattern:

4.1 The entire course of study is of four semesters. During the first and second semesters the student has to undergo course work and during the third and fourth semesters the student has to carry out project work.

4.2 The student shall be eligible to appear for the End Examination in a subject, but absent at it or has failed in the End Examination may appear for that subject at the supplementary examination.

Table 1: Credits

Subject	Semester			
	Periods /Week	Credits	Internal marks	External marks
Theory	04	04	40 (25 Internal Test+15 Assignment)	60
Practical	03	02	50	50
Seminar		02	100	
Comprehensive Viva – voce 1		02		50
Comprehensive Viva - voce 2		02		50
Project		12		

Table2: Course pattern

Semester	No.of Subjects	Number of Labs	Total credits	
First	04-Subjects 01-Elective 01-MOOC/Elective	 02 - Labs Comprehensive Viva -1	04X4=16 01X4=04 01X4=04 02X2=04 01X2=02	30
Second	04-Subjects 01-Elective 01-MOOC/Elective	 02 - Labs Comprehensive Viva -2	04X4=16 01X4=04 01X4=04 02X2=04 01X2=02	30
Third	Seminar(3^{rd} semester) Intermediate Evaluation of Project work(3^{rd} semester)			02 04
Fourth	Project Work			08
			Total credits	**74**

5.0 Attendance:

5.1 The candidate shall be deemed to have eligibility to write end semester examinations, if he has secured a minimum of 75% of attendance in aggregate of all the subjects.

5.2 Condonation of shortage of attendance up to 10%, i. e. 65% and above and below 75% may be given by the College academic committee consisting of Principal, Head of the Department and a senior faculty member.

5.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence.

5.4 Shortage of attendance below 65% shall in no case be condoned.

5.5 The candidate shall not be promoted to the next semester unless he fulfils the attendance requirements of the previous semester.

5.6 Attendance in each subject will be recorded in the marks memo.

5.7 The attendance in each subject will be recorded in the Marks memo.

6.0 Evaluation:

6.1 For theory subjects the distribution shall be 40 marks for Internal Evaluation (25 marks for Internal test and 15 marks for assignments/ field work) and 60 marks for the End-Examination.

6.2 Each Internal Test question paper shall contain 5 questions, of which the First question is compulsory and three questions are to be answered from the remaining four. Compulsory question carries 10 marks (It contains 5 short answer questions). The remaining 3 questions carry 5 marks each. Each question shall have a,b,c.... parts. The duration of internal test will be for 2 hours. First test to be conducted in 3 units in the middle of the semester and second test to be conducted in the remaining 3 units of each subject at end the semester. There shall be two assignments in each subject (problem based/ field work) for the award of 15 marks so that internal component (marks) will be 40 marks (25 marks for internal test+15 marks for assignments / field work). For awarding of 25 Internal marks the performance of the student in two internal examinations conducted will be considered by giving a weightage of 0.75 for the better score and 0.25 for the other score.

6.3 The End Examination question paper will have 7 questions and students have to answer 5 questions. However, the first question is compulsory and it consists of 6 short answer questions, each carrying 2 marks. The next 4 questions are to be answered from the remaining 6 questions and each carries 12 marks. Each 12 marks question shall have a, b, c ..parts.

6.4 Elective subjects will commence from 1st semester. Out of the electives offered in 1st / 2nd semester, one elective will be MOOC / Electives offered by the department. Any student who is interested can opt for the MOOC/ Electives offered by the department and acquire the required credits. Even if the student opts MOOC, he has to write two internal tests besides the end examination conducted by the institute like other subjects. However, he has to obtain the certificate from the organization in which he has registered. Any MOOC selected

by the student should be of more than 45 hours duration and also from the reputed organization. Attendance of the student who has opted for MOOC will be taken from the remaining subjects and labs only in that semester while finalizing the attendance for fulfilling the minimum requirements of attendance for promotion to next semester. Attendance will not be recorded for MOOC. Where ever MOOC is opted by the student, the evaluation procedure will be similar to any subject offered by the department.

6.5 For practical subjects, 50 marks shall be for the End Semester Examinations and 50 marks will be for internal evaluation based on the day-to-day performance.Laboratory examination for M.Tech.. Course shall be conducted with two Examiners, one of them being Laboratory Class Teacher and second Examiner shall be outside from the institute (External examiner).

6.6 Student has to undergo a comprehensive viva pertaining to his specialization which carries 50 marks in each semester. He has to secure 50% marks to obtain required credits. Comprehensive viva will be conducted at the end of 1st and 2nd semester by the committee consisting of HOD, senior faculty member and external Examiner from outside the institute. For this, HOD of the Department shall submit a panel of 4 Examiners, who are eminent in that field. One from the panel will be selected by the principal of the institute as external Examiner for comprehensive viva.

6.7 For Seminar 100 marks shall be for internal evaluation. The candidate has to secure a minimum of 50 marks to be declared successful. The assessment will be made by a board consisting of HOD and two internal experts at the end of 3rd semester.

6.8 The candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Examination and Internal evaluation taken together.

6.9 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.0), he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the course when next offered or do any other specified subject as may be required.

7.0 Re-registration for improvement of Internal marks:

Following are the conditions to avail the benefit of improvement of internal marks.

7.1 The candidate should have completed the course work and obtained examinations results for 1st&2nd semesters.

7.2 He should have passed all the subjects for which the internal marks secured are more than 50%.

7.3 Out of the subjects the candidate has failed in the examination due to Internal marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of three Theory subjects for Improvement of Internal marks.

7.4 The candidate has to re-register for the chosen subjects and fulfil the academic requirements as and when they are offered.

7.5 For each subject, the candidate has to pay a fee equivalent to one tenth of the semester tuition fee and the amount is to be remitted in the form of D. D. in favour of the Principal, RGMCET payable at RGMCET, Nandyal branch along with the requisition through the HOD of the respective Department.

7.6 In case of availing the Improvement of Internal marks, the internal marks as well as the End Examinations marks secured in the previous attempt (s) for the re-registered subjects stand cancelled.

8.0 Evaluation of Project / Dissertation work :

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Department.

8.1 Registration of Project work: The candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses (theory and practical courses of 1st& 2ndSem)

8.2 An Internal Department Committee (I.D.C.) consisting of HOD, Supervisor and One Internal senior expert shall monitor the progress of the project work.

8.3 The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

8.4 The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C. before submission of the Project Report.

8.5 The candidate shall be allowed to submit the thesis/dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva voce examination of the project. The viva - voce examination may be conducted once in two months for all the candidates submitted during that period.

8.6 Three copies of the Thesis/Dissertation certified in the prescribed form by the supervisor & HOD shall be submitted to the institute.

8.7 The Department shall submit a panel of 4 experts for a maximum of 4 students at a time. However, the thesis/dissertation will be adjudicated by the board consists of HOD, concerned supervisor and one external Examiner from other institute nominated by the principal from a panel of Examiners submitted by the Department HOD to the Controller of Examinations.

8.8 If the report of the board is favourable in viva voce examination, the board shall jointly report candidates work as:

1. Good
2. Satisfactory
3. Not satisfactory

If the report of the viva voce is not satisfactory the candidate will retake the viva voce examination after three months. If he fails to get a satisfactory report at the second viva voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the thesis.

9.0 Award of Degree and Class:

After the student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following classes:

Table 3: Award of division

Class Awarded	**% of marks to be secured**	Division/ Class	CGPA	From the aggregate marks secured from the 74 Credits.
First Class with Distinction	70% and above	First Class With Distinction	≥ 7.5	
First Class	Below 70% but not less than 60%	First Class	6.5 *and* < 7.5	
Second Class	Below 60% but not less than 50%	Second Class	≥ 5.5 *and* < 6.5	

(The marks in internal evaluation and End Examination shall be shown separately in the marks memorandum)

10.0 *Grading:*

After each subject is evaluated for 100 marks, the marks obtained in each subject will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student falls.

Table 4: Conversion into Grades and Grade points assigned

Range in which the % of marks in the subject fall	Grade	Grade point Assigned	Performance
90 to 100	O	10	Outstanding
80 to 89.9	A^+	09	Excellent
70 to 79.9	A	08	Very good
60 to 69.9	B^+	07	good
50 to 59.9	B	06	Pass
<50	F	00	Fail
Ab	AB	00	Fail

10.1 Requirement for clearing any subject: The students have to obtain a minimum of 40% in End Examination and they have to score minimum of 50% marks from Internal and external exam marks put together to clear the subject. Otherwise they will be awarded fail grade.

10.2 F is considered as a fail grade indicating that the student has to reappear for the end supplementary examination in that subject and obtain a non fail grade for clearing that subject.

10.3 To become eligible for the award of degree the student must obtain a minimum CGPA of 6.0.

11.0 Supplementary Examinations:

Apart from the regular End Examinations the institute may also schedule and conduct supplementary examinations for all subjects for the benefit of students with backlogs. Such students writing supplementary examinations as supplementary candidates may have to write more than one examination per day. The student is not permitted to improve his performance in any subject in which he has obtained pass grade.

12.0 *Grade Point Average (GPA) and Cumulative Grade Point Average(CGPA)*

The Grade Point Average (GPA) for each semester and Cumulative Grade Point Average (CGPA) up to any semester are calculated as follows:

i) Semester Grade Point Average will be computed as follows:

$$GPA = \frac{\sum_1^n C_i \times GP_i}{\sum_1^n C_i}$$

Where, n is the number of subjects in that semester. C_i is Credits for the subjects. GP_i is the grade point obtained for the subject and the summation is over all the subjects in that semester.

ii) A Cumulative Grade Point Average (CGPA) will be computed for

every student at the end of each semester. The CGPA would give the cumulative performance of The student from the first semester up to the end of the semester to which it refers and is calculated as follows

$$CGPA = \frac{\sum_1^m GPA_j \times TC_i}{\sum_1^m TC_j}$$

Where 'm' is the number of semester under consideration.TC_j the total number of credits for a j^{th}semester and GPA_j is the Grade Point Average of the j^{th} semester. Both GPA and CGPA will be rounded off to the second digit after decimal and recorded as such.

While computing the GPA / CGPA the subjects in which the student is awarded zero grade points will also be included.

13.0 Grade Sheet:

A grade sheet (Memorandum) will be issued to each student indicating his performance in all subjects of that semester in the form of grades and also indicating the GPA and CGPA.

14.0 Transcripts:

After successful completion of prerequisite credits for the award of degree a Transcript containing performance of all academic years will be issued as a final record. Duplicate transcripts will also be issued if required after the payment of requisite fee and also as per norms in vogue.

15.0 Minimum Instruction Days:

The minimum instruction days for each semestershall be 95 clear instruction days excluding the days allotted for tests/examinations and preparation holidays declared if any.

16.0 Amendment of Regulations:

The college may, from time to time, revise, amend or change the regulations, scheme of examinations and syllabi. However the academic regulations of any student will be same throughout the course of study in which the student has been admitted.

17.0 Transfers

There shall be no branch transfers after the completion of admission process.

18.0 Withholding of results:

If the candidate has not paid any dues to the institute or if any case of in-discipline is pending against him, the result of the candidate will be withheld and he will not be allowed for the next semester. The issue of the degree is liable to be withheld in such cases.

19.0 Transitory Regulations:

Candidates who have discontinued or have been detained for want of attendance are eligible for admission to the same or equivalent subjects as and when subjects are offered, subject to 2.0 and 5.0.

20.0 Rules of Discipline:

20.1 Any attempt by any student to influence the teachers, Examiners, faculty and staff of Examination section for undue favours in the exams, and bribing them either for marks or attendance will be treated as malpractice cases and the student can be debarred from the college.

20.2 When the student absents himself, he is treated as to have appeared and obtained zero marks in that subject (s) and grading is done accordingly.

20.3 When the performance of the student in any subject (s) is cancelled as a punishment for indiscipline, he is awarded zero marks in that subject (s).

20.4 When the student's answer book is confiscated for any kind of attempted or suspected malpractice, the decision of the Chief Superintendent is final.

21.0 General:

21.1 The Academic Regulations should be read as a whole for the purpose of any interpretation.

21.2 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the College Academic Council is final.

21.3 The Institute may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Institute.

21.4 *Where the w*ords "he", "him", "his", occur in the regulations, they include "she", "her", "hers".

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

COURSE STRUCTURE

M.TECH, I-SEMESTER

Code	Subject	Scheme of instruction periods/week		Credits	Scheme of Examination		
		Theory	Practical		Internal	External	Total
D0601151	Digital System Design	4	-	4	40	60	100
D0602151	Embedded System Concepts	4	-	4	40	60	100
D0603151	Advanced Computer Architecture	4	-	4	40	60	100
D0604151	Advanced Data Communications	4	-	4	40	60	100
	ELECTIVE-I	4	-	4	40	60	100
D0605151	Image & Video Processing						
D0606151	TCP/IP & ATM NETWORKS						
D0607151	SOC Architecture						
	ELECTIVE-II/MOOC	4	-	4	40	60	100
D0608151	Experts systems						
D0609151	VLSI Technology						
D0610151	Algorithms for VLSI Design Automation						
D0611151	FPGA/CPLD Lab	-	3	2	50	50	100
D0612151	Image Processing Lab	-	3	2	50	50	100
D0613151	Comprehensive Viva-I	-	-	2	-	50	50
	Total	24	6	30	340	510	850

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COURSE STRUCTURE
M.TECH, II-SEMESTER

Code	Subject	Scheme of instruction periods/week		Credits	Scheme of Examination		
		Theory	Practical		Internal	External	Total
D0614152	Micro Computer Systems Design	4	-	4	40	60	100
D0615152	Neural Networks & Applications	4	-	4	40	60	100
D0616152	Design of Fault Tolerant Systems	4	-	4	40	60	100
D0617152	Systems Programming	4	-	4	40	60	100
	ELECTIVE-III	4	-	4	40	60	100
D0618152	Embedded 'C'						
D0619152	Wireless Sensor Networks						
D0620152	Network Security & Cryptography						
	ELECTIVE-IV/MOOC	4	-	4	40	60	100
D0621152	System Modeling and Simulation.						
D0622152	Statistical Signal Processing						
D0623152	FPGA Architecture & Applications						
D0624152	Embedded Systems Programming Lab	-	3	2	50	50	100
D0625152	Neural Networks using MATLAB	-	3	2	50	50	100
D0626152	Comprehensive Viva-II	-	-	2	-	50	50
	Total	24	6	30	340	510	850

M.TECH, III-SEMESTER & IV-SEMESTER

Code	Subject	Credits	Internal Marks	External Marks	Total
D0627153	Seminar (End of III Semester)	2	100	-	100
D0628154	Project work	12	-	-	-

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M.Tech I-Sem (DSCE) T 4 C 4

(D0601151) DIGITAL SYSTEMDESIGN

UNITI

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reductionofstatetables,stateassignments.

UNITII

SEQUENTIALCIRCUITDESIGN:designofIterativecircuits,designofsequentialcircuitsusingROMsandPLAs, sequentialcircuitdesignusingCPLD,FPGAs.

UNITIII

FAULTMODELING:Faultclassesandmodels,stuckatfaults,bridgingfaults,transitionandintermittentfaults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique,Booleandifferencemethod,Kohavialgorithm.

UNITIV

TESTPATTERNGENERATION:D–algorithm,
PODEM,Randomtesting,transitioncounttesting,Signature analysisandtestingforbridgingfaults.

UNITV

FAULTDIAGNOSISINSEQUENTIALCIRCUITS:Stateidentificationandfaultdetectionexperiment.Machine identification, Design of fault detection experiment.
ASYNCHRONOUS SEQUENTIALMACHINE: Fundamental modemodel, flowtable, statereduction, minimal closedcovers,races,cyclesandhazards.

UNITVI

PROGRAMMING LOGIC ARRAYS: Design using PLA's, PLA minimization and PLA folding, Faultmodels,TestgenerationandTestablePLAdesign.

TEXTBOOKS:

1. Kohavi – "Switching & finite Automata Theory" (TMH), 2nd edition.
2. N. Biswas – "Logic Design Theory" (PHI), 2006.
3. OlmanBalabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition 2004.

REFRENCES:

1. M.Abramovici, M.A.Breues, A.D. Friedman – "Digital System Testing and Testable Design", Jaico Publications, 2008.
2. Charles H. Roth Jr. – "Fundamentals of Logic Design", 5th edition, 2005, Singapore Publications.
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – John Wiley & Son's publications, 4th Edition, 1993.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, I-Sem(DSCE) T C

4 4

(D0602151) EMBEDDED SYSTEM CONCEPTS

(Common to DSCE & ES)

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems.

UNIT II

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems: I^2C bus, CAN bus. Communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT III

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space.

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique.

UNIT IV

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes.

UNIT V

INSTRUCTION SETS: Introduction, preliminaries, ARM processor: Processor and Memory organization, data operations, flow of control, simple examples. SHARC processor: Memory organization, data operations, flow of control, Simple examples

UNIT VI

SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications: Control-Oriented specification languages, advanced specifications. system analysis and architecture design, quality assurance techniques.

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes, etc.

TEXT BOOKS:

1. Computers as a component: principles of embedded computing system design- wayne wolf, reprint 2009.
2. An embedded software premier: David E. Simon, 2007, 4th edition.
3. Rajkamal, “Embedded systems: Architecture, Programming and Design”, TMH

REFERENCES:

1. Embedded real time systems programming-Sri ram V Iyer, PankajGupta, TMH, 2004.
2. Embedded system design- A unified hardware/software introduction- frank vahid, tony D. Givargis, John Willey, 2002.
3. Embedded/real time systems-KVKK Prasad, Dreamtech press, 2005

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M.Tech, I-Sem(DSCE) T C

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(D0603151) ADVANCED COMPUTER ARCHITECTURE

(Common to DSCE & ES)

UNIT I

FUNDAMENTALS OF COMPUTER DESIGN: Technology trends, cost, price and their trends, cost of an integrated circuits, measuring and reporting performance, quantitative principles of computer design-Amdahl's law, CPU performance equation.

UNITII

INSTRUCTIONSETPRINCIPLESANDEXAMPLES:

classifyinginstructionset,memoryaddressing,typeandsizeofoperands, addressingmodesforsignalprocessing, operationsintheinstructionset-instructionsforcontrolflow-encodingan instructionset.-theroleofcompiler.

UNITIII

INSTRUCTIONLEVELPARALLELISM(ILP): Instruction-level parallelism concepts and challenges, Overcomingdatahazards, dynamic scheduling using tomasulo's approach, reducingbranchcosts, highperformanceinstruction delivery, hardwarebasedspeculation,limitation of ILP, ILPSOFTWAREAPPROACH:Basic CompilerTechniques,Static BranchProtection,VLIWApproach,H.WsupportformoreILPat compiletime, conditional or predicated instructions, compiler speculation with hardware support,H.WversesS.Wsolutions.

UNITIV

MEMORY HIERARCHY DESIGN: review of caches, cache performance,reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

MULTIPROCESSORSANDTHREADLEVELPARALLELISM:a taxonomy of parallel architecture, symmetricsharedmemoryarchitectures-basic schemes for enforcing coherence, snooping protocols,distributedsharedmemory, Synchronization,multi-threading.

UNITV

STORAGESYSTEMS: Types of storage devices,Buses-connecting I/O devices to CPU/memory,RAID,errorsandfailures in real systems,bench marks of storage performance and availability,designing aI/O system.

UNITVI

INTERCONNECTIONNETWORKSANDCLUSTERS: Interconnectionnetworkmedia, practicalissuesi ninterconnectingnetworks-connecting the network to the computer, standardization, message failure tolerance, node failure tolerance, examples of interconnection networks,clusters,designing a cluster.

TEXTBOOKS:

1. John. Hennessy &DavidA.PattersonMorganKufmann, "ComputerArchitectureAquantitativeapproach", 3rd edition (AnImprintofElsevier), 2003.

REFERENCES:

1. KaiHwangandA. Briggs, "ComputerArchitectureandparallelProcessing", InternationalEditionMcGraw-Hill, 1985.
2. DezsoSima,TerenceFountain,PeterKacsuk, "AdvancedComputerArchitectures", Pearson, 2008.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, I-Sem(DSCE) T C
4 4

(D0604151) ADVANCED DATA COMMUNICATIONS

UNIT I

DIGITAL MODULATION: Introduction, Information Capacity Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK, Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

BASIC CONCEPTS OF DATA COMMUNICATIONS, INTERFACES AND MODEMS:Data Communication, Components, Networks, Distributed Processing, Network Criteria-Applications, Protocols and Standards, Standards Organizations, Regulatory Agencies.

UNIT II

Line Configuration- Point-to-point- Multipoint, Topology, Mesh, Star, Tree, Bus, Ring, Hybrid Topologies, Transmission Modes, Simplex, Half duplex- Full Duplex, Categories of Networks-LAN, MAN, WAN and Internetworking, Digital Data Transmission- Parallel and Serial, DTE-DCE Interface-Data Terminal Equipment, Data Circuit-Terminating Equipment, Standards EIA 232 Interface, Other Interface Standards, Modems- Transmission Rates.

UNIT III

ERROR DETECTION AND CORRECTION: Types of Errors- Single- Bit Error, CRC (Cyclic Redundancy Check), Performance, Checksum, Error Correction- Single-Bit Error Correction, Hamming Code.

UNIT IV

DATA LINK CONTROL: Stop and Wait, Sliding Window Protocols.

DATA LINK PROTOCOLS: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocol- Binary Synchronous Communication (BSC) - BSC Frames- Data Transparency, Bit Oriented Protocols, HDLC, Link Access Protocols.

UNIT V

SWITCHING*:* Circuit Switching- Space Division Switches- Time Division Switches, TDM Bus, Space and Time Division Switching Combinations, Public Switched Telephone Network, Packet Switching- Datagram Approach- Virtual Circuit Approach, Circuit Switched Connection Versus Virtual Circuit Connection, Message Switching.

MULTIPLEXING:Time Division Multiplexing (TDM), Synchronous Time Division Multiplexing, Digital Hierarchy, Statistical Time Division Multiplexing.

UNIT VI

MULTIPLE ACCESS: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Detection (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization- Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), - Code - Division Multiple Access (CDMA).

TEXT BOOKS:

1) B. A.Forouzan, “Data Communication and Computer Networking”, 3rd ed., TMH, 2008.
2) W. Tomasi, “Advanced Electronic Communication Systems”, 5 ed., PEI2008.

REFERENCES:

1) Prakash C. Gupta, “Data Communications and Computer Networks”, PHI, 2006.
2) William Stallings, “Data and Computer Communications”, 8th ed., PHI 2007.
3) T. Housely, “Data Communication and Tele Processing Systems”, 2nd Edition, BSP, 2008.
4) Brijendra Singh, “Data Communications and Computer Networks”, 2nd ed., PHI 2005.

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Autonomous

DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, I-Sem(DSCE) T C
4 4

(D0605151) IMAGE & VIDEO PROCESSING

(ELECTIVE-I)

UNIT I

IMAGE REPRESENTATION: Gray scale and colour Images, image sampling and quantization. Two dimensional orthogonal transforms: DFT, WHT, Haar transform, KLT, DCT.

UNIT II

IMAGE ENHANCEMENT: Enhancement by point processing, histogram-based processing, homomorphic filtering, Filters in spatial and frequency domains (Smoothing & Sharpening filters).

UNIT III

IMAGE RESTORATION: Degradation Models, PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering, Constrained restoration.

IMAGE SEGMENTATION: Pixel classification, Bi-level Thresholding, Multi-level Thresholding, Adaptive Thresholding, Edge detection, Hough transform, Region based segmentation.

UNIT IV

FUNDAMENTAL CONCEPTS OF IMAGE COMPRESSION: Need for compression, classification of redundancy in images, Compression models, classification of image compression schemes, dictionary based compression.

LOSSLESS COMPRESSION: Huffman Coding, Arithmetic coding, Bit plane coding, Run length coding, Lossy compression: Transform coding, Image compression standards.

UNIT V

VIDEO FORMATION, PERCEPTION, REPRESENTATION AND SAMPLING: Video capture and display, analog video raster, analog color television systems, digital video, basics of multi dimensional continues space signals and systems, discrete space signals and systems, basics of lattice theory, sampling over lattices, sampling of video signals, filtering operations in cameras and display devices, sampling rate conversion of video signals.

UNIT VI

TWO DIMENSIONAL MOTION ESTIMATION: Optical flow, general methodologies, pixel based motion estimation, block matching algorithm, deformable block matching algorithms, mesh based motion estimation, application of motion estimation in video coding.

TEXT BOOKS:

1. R. C. Gonzalez, R. E. Woods, "Digital Image Processing", Pearson Education. 2nd edition, 2002.
2. S.Jayaraman, S.Esakkirajan&T.Veera Kumar "Digital Image Processing", Tata McGraw Hill, 2009.
3. Yao Wang, JormOstermann and Ya Qin Zhang "Video Processing and Communications" PHI, 2002.

REFERENCES:

1. W. K. Pratt, "Digital image processing", Prentice Hall, 1989.
2. A. M. Tekalp, "Digital Video Processing", Prentice-Hall, 1995.
3. A. Bovik, "Handbook of Image & Video Processing", Academic Press, 2000.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, I-Sem (DSCE) T 4 C 4

(D0606151) TCP/IP AND ATM NETWORKS

(ELECTIVE -I)

UNIT –I

INTERNET PROTOCOL: Internetworking, IPV4, IPV6, Transition from IPV4 to Ipv6.Process to process delivery, UDP, TCP andSCTP.

UNIT –II

CONGESTION CONTROL AND QUALITY OF SERVICE: Data traffic, congestion, congestion control, two examples, Quality of Service, Techniques to improveQOS, Integrated services, and Differentiated services.

UNIT –III

QUEUE MANAGEMENT: Passive-Drop-tail, Drop front, Random drop, Active –Early Random drop,Random Early Detection, Design Goals, ATM Architecture, Switching, Switch Fabric, ATM Layers, Service Classes, ATM Application

UNIT-IV

SPREAD SPECTRUM: Introduction, Basic Concept, Protection against Jamming, Spreading Codes (PN-Sequence),
Generation, Properties, Types of Spread Spectrum Techniques, Application Of Spread Spectrum.

UNIT –V

X.25:- X.25 Layers, X.21 protocol,**Frame Relay:-**Introduction, Frame relay Operation, Frame relay Layers, Congestion Control, LeakyBucket algorithm.

UNIT –VI

INTERCONNECTION NETWORKS: Introduction, Banyan Networks, Properties, Crossbar Switch, Three Stage Class Networks,Rearrangeble Networks, Folding Algorithm, Benes Networks, Lopping Algorithm, Bit AllocationAlgorithm.**SONET/SDH:-**Synchronous Transport Signals, Physical Configuration, SONET Layers, SONETFrame.

TEXT BOOKS:

1. Data communication and Networking. -B.A. Forouzen, 4th Edition TMH
2. TCP/IP Protocol Suit - B.A. Forouzen, 4th Edition TMH

REFERENCE BOOKS:

1. Wireless Communication System -Abhishekyadav –University Sciences Press, 2009
2. Wireless Digital Communications -Kamilo Feher-1999 PHI
3. High Performance TCP-IP Networking -Mahaboob Hassan -Jain Raj-PHI
4. Data Communication & Networking -B. A. Forouzan 2nd Edition TMH
5. ATM Fundamentals – N.N.Biswas -Adveture book Publishers-1998

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, I-Sem (DSCE) T 4 C 4

(D0607151) SYSTEM ON CHIP ARCHITECTURE

(ELECTIVE -I)

UNIT –I:

INTRODUCTION TO THE SYSTEM APPROACH: System Architecture, Components of the system, Hardware & Software, Processor Architectures,Memory and Addressing. System level interconnection, An approach for SOC Design, SystemArchitecture and Complexity.

UNIT –II:

PROCESSORS: Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT –III:

MEMORY DESIGN FOR SOC: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT -IV:

INTERCONNECT CUSTOMIZATION AND CONFIGURATION: Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

UNIT-V:

SOC CUSTOMIZATION: Anoverview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

UNIT –VI:

APPLICATION STUDIES / CASE STUDIES:SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEGcompression.

TEXT BOOKS:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely IndiaPvt. Ltd.
2. ARM System on Chip Architecture – Steve Furber –2nd Ed., 2000, Addison WesleyProfessional.

REFERENCE BOOKS:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004,Springer
2. Co-Verification of Hardware and Software for ARM System on Chip Design (EmbeddedTechnology) – Jason Andrews – Newnes, BK and CDROM.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, I-Sem (DSCE) T 4 C 4

(D0608151) EXPERT SYSTEMS

(ELECTIVE –II/MOOC)

(Common to DSCE & ES)

UNIT I

KNOWLEDGE REPRESENTATION AND ISSUES: Notational systems: Trees, graphs, hierarchies, propositional and predicate logics, frames, semantics networks, constraints, conceptual dependencies, database, knowledge discovery in databases (KDD).

UNIT II

SEARCH: State-space representations, Depth-first, breadth-first, heuristic search, Planning and game playing, Genetic algorithms.

UNIT III

LOGICAL REASONING AND PROBABILISTIC REASONING: Predicate, Calculus resolution, completeness, and strategies, Unification, Prolog, monotonic and non-monotonic reasoning.

UNIT IV

EXPERT SYSTEMS: Probabilistic inference networks, Fuzzy inference rules, Bayesian rules. Dempster-Shafer Calculus.Expert Systems, Organization, tools, limits, examples.

UNIT V

LEARNING AND COMMON SENSANE REASONING: Robot actions, strips, triangle tables, case based reasoning, spatial and temporal formalisms.

UNIT VI

Knowledge acquisition, classification rules, self directed systems.

NEURAL NETWORKS**:** Principles, biological analogies, Training (techniques and errors), Recognition.

TEXT BOOKS:

1. Charniak .E,And McDermott .D., ”Intoduction to Artificial intelligence”, Addison-Wesley, 1987
2. Giarratano.J.,And Riley G., ”Expert Systems principles an Programming” PWS-KENT,1989

REFERENCES:

1. Introduction to expert systems by Peter Jackson, 3rd edition, Addison-Wesley, 1999.
2. Expert systems: Principles and Programming, by Joseph C.Giarrantano, Gary D.Riley, Gary Riley, 4th edition, Cengage learning, 2004.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, I-Sem(DSCE) T C

4 4

(D0609151)VLSI TECHNOLOGY

(ELECTIVE II/MOOC)

(Common to DSCE & ES)

UNIT I

INTRODUCTION TO MOS TECHNOLOGY & BASIC ELECTRICAL PROPERTIES OF MOS: Overview of VLSI Design Methodologies**,** VLSI Design flow, Styles of VLSI Design, CAD Technology, MOS Transistors and its Trends, I_{ds}-V_{ds} Relationships, Threshold voltage V_t, g_m, g_{ds} and W_o, Pass Transistor, MOS Z_{pu}/Z_{pd}, MOS Transistor circuit model.

UNIT II

CMOS Design: CMOS Logic, Static Complementary gates, Transmission Gate Logic Design, Bi-CMOS Inverters, Latch-up in CMOS circuits.

UNIT III

LAYOUT DESIGN AND TOOLS:, Switch Logic, Alternative Gate Circuits, Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

UNIT IV

COMBINATIONAL LOGIC NETWORKS & INTERCONNECTS: Layouts, Simulation, Network Delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT V

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT VI

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, Architecture for Low Power, SOCs and Embedded CPU Architecture Testing.

TEXT BOOKS:

1. K. Eshraghianetal.(3 authors), “Essentials of VLSI Circuits and Systems”, PHI of India Ltd., 2005
2. Wayne Wolf, “Modern VLSI Design”, 3/E, Pearson Education, fifth Indian Reprint, 2005.
3. Sung-Mo Kang and Yusuf Leblebici, “CMOS Digital Integrated Circuits Analysis and Design” TATA McGraw Hill,3rdEdition, 2003.

REFERENCES:

1. N.H.E Weste, K.Eshraghian, “Principals of CMOS Design”, Addison Wesley, 2nd Edition.
2. Ken Martin, “Digital Integrated Circuits Design” oxford University Press, 2nd impression, 2005.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, I-Sem (DSCE) T 4 C 4

(D0610151) ALGORITHMS FOR VLSI DESIGN AUTOMATION

(ELECTIVE-II/MOOC)

(COMMON TO DSCE & ES)

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT IV

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT VI

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", Wiley Student Edition, John wiley& Sons (Asia) Pvt. Ltd., 1999.
2. NaveedSherwani, "Algorithms for VLSI Physical Design Automation", 3rd edition, Springer International Edition, 2005.

REFERENCES:

1. Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", Wiley, 1993.
2. Wayne Wolf, "Modern VLSI Design: Systems on silicon", Pearson Education Asia, 2nd Edition, 1998.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, I-Sem(DSCE) P C

3 2

(D0611151) FPGA/CPLD LAB

(Common to DSCE & ES)

Minimum of 10 experiments to be conducted

1. Simulation and Verification of Logic Gates.
2. Simulation and Verification of 74x138.
3. Simulation and Verification of 74x151.
4. Simulation and Verification of 74x157.
5. Simulation and Verification of 74x280.
6. Simulation and Verification of 74x148.
7. Simulation and Verification of 74x74.
8. Simulation and Verification of 74x163.
9. Simulation and Verification of 74x194.
10. Design, Simulation of Counters- Ring Counter, Johnson Counter, Mod counters.
11. FiniteState Machine- Mealy and Moore Machines.
12. Design, Simulation and verification of Dual Priority encoder.
13. Design, Simulation and verification of Floating point encoder.

Implementation of all the Design using FPGA and CPLD Devices.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, I-Sem(DSCE) P C

3 2

(D0612151) IMAGE PROCESSING LAB

Minimum of 10 experiments/Programmes to be conducted

1. Basic operations on images.
2. Generation of basis functions for different transforms.
3. Operation of various transforms on images.
4. Verification of 2D-DFT properties.
5. Histogram equalization and adaptive histogram equalization.
6. Image enhancement in spatial domain.
7. Image enhancement in frequency domain.
8. Image restoration using inverse filter and wiener filter.
9. Edge detection using various operators.
10. Detecting a cell using image segmentation.
11. Different operation on color images.
12. Image compression techniques.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem(DSCE) T 4 C 4

(D0614152) MICRO COMPUTER SYSTEMDESIGN

UNIT I

REVIEW OF 8086 PROCESSOR: Architecture, Register organization, Addressing Modes and Instruction Set (Brief treatment only), Difference between 8086 and 8088 with rest to pin structures.

UNITII

THE 80286 MICRO PROCESSORS: Architecture, Register Organization, Addressing Modes and instruction sets of 80286 (brief treatment only)

UNITIII

THE 80386, AND 80486 MICRO PROCESSORS: Architectural features, Register Organization, Memory management, Virtual 8086 mode, The Memory Paging Mechanism, Pin Definitions of 80386 and 80486 (brief treatment).

UNITIV

THE PENTIUM AND PENTIUM PRO PROCESSORS: The Memory System, Input/output system, Branch Prediction Logic, Cache Structure, Pentium Registers, Serial Pentium pro features.

THE PENTIUM IV AND DUAL CORE MICRO PROCESSORS: Architecture, Special Registers and Pin Structures (brief treatment only)

UNIT V

I/O PROGRAMMING: Fundamentals of I/O, Considerations Programmed I/O, Interrupt I/O, Block Transfers and DMA, I/O Design Example.

MULTI PROCESSOR SYSTEMS: Interconnection Topologies, Software Aspects of Multi microprocessors systems, Numeric processor 8087, I/O processor 8089, Bus arbitration and control, Tightly coupled and loosely coupled systems.

UNIT VI

ARITHMETIC COPROCESSOR, MMX AND SIMD TECHNOLOGIES: Data formals for Arithmetic Coprocessor, Internal Structure of 8087 and Advanced Coprocessors. Instruction Set (brief treatment).

TEXTBOOKS:

1) Barry, B. Brey, "The Intel Microprocessors,"8th Edition Pearson Education, 2009.
2) A.K. Ray and K.M. Bhurchandi, "Advanced Microprocessor and Peripherals" 2nd edition, TMH, 19th reprint, 2011.

REFERENCES:

1. YU-Chang, Glenn A. Gibson, "Micro Computer Systems: The 8086/8088 Family Architecture, programming and design, PHI, 1986.
2. Programming and Design" 2nd Edition, Pearson Education, 2007
3. Douglas V. Hall, "Microprocessors and Interfacing," Special Indian Edition, 2006.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem(DSCE) T 4 C 4

(D0615152) NEURAL NETWORKS & APPLICATIONS

UNIT I

FUNDAMENTAL CONCEPTS AND MODELS OF ARTIFICIAL NEURAL SYSTEMS: Structure of Biological Neuron, McCulloch-Pitts Neuron Model, Neuron Modeling for Artificial Neural Systems,Models of Artificial Neural Networks: Feedforward Network and feedback Network. Neural Processing, Learning: Supervised and Unsupervised learning.

Neural Network Learning Rules:Hebbian Learning Rule, Perceptron Learning Rule, Delta Learning Rule, Widrow-Hoff Learning Rule, Correlation Learning Rule, Winner–Take-All Learning rule, OutStar Learning Rule.

UNIT II

SINGLE- LAYER PERCEPTRON CLASSIFIERS: Classification Model, Features, and Decision Regions, Discriminant Functions, Linear Machine and Minimum Distance Classification, Training and classification using the discrete perceptron, Single Layer Continuous Perceptron Networks for Linearly Separable Classifications, Multicategory Single Layer Perceptron Networks.

UNIT III

MULTILAYER FEEDFORWARD NETWORKS: Linearly Nonseparable Pattern Classification, Delta LearningRule for Multiperceptron Layer,Generalized Delta Learning Rule, Feed forward Recall and Error BackPropagation Training: Feedforward Recall, Error Back-Propagation Training.

UNIT IV

SINGLE-LAYER FEEDBACK NETWORKS: Basic concepts of Dynamical systems. Mathematical Foundation of Discrete-Time Hopfield Networks.Mathematical Foundation of Gradient-Type Hopfield Networks.

UNIT V

ASSOCIATIVE MEMORIES: Basic concepts, Linear associator, Basic concepts of Recurrent Auto associative memory: Retrieval algorithm, Storage algorithm, Bidirectional Associative Memory.

UNIT VI

MATCHING AND SELF-ORGANIZING NETWORKS: Hamming net and MAXNET, Unsupervised Learning of Clusters, Clustering and Similarity Measures, Winner-Take-All Learning, Recall Mode, Initialization of Weights, Counter propagation network, Feature mapping, Self organizing feature maps.

TEXT BOOKS

1. J.M.Zurada: Introduction to Artificial Neural Systems, Jaico Publishers, 8th Impression, 2005.
2. Dr. B. Yagananarayana, Artificial Neural Networks, PHI, New Delhi, 2005.

REFERENCES

1. KishanMehrotra, Chelkuri K. Mohan, Sanjay Ranka: Elements of Artificial Neural Networks, Penram International, 1997.
2. Introduction Neural Networks Using MATLAB 6.0 - by S.N. Sivanandam, S. Sumati, S. N. Deepa,1/e, TMH, New Delhi, 2006.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem(DSCE) T 4 C 4

(D0616152) DESIGN OF FAULT TOLERANT SYSTEMS

UNIT I

BASIC CONCEPTS: Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and Mean time between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.

UNIT II

FAULT TOLERANT DESIGN: Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self-purging redundancy, Sift out redundancy (SMR), SMR Configuration, Use of error correcting code, Time redundancy and software redundancy.

UNIT III

SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

FAIL SAFE DESIGN: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, totally self-checking PLA design.

UNIT IV

DESIGN FOR TESTABILITY FOR COMBINATIONAL CIRCUITS: Basic concepts of testability, controllability and observability, the Reed Muller's expansion technique, OR-AND-OR design, use of control and syndrome testable design.

UNIT V

SIGNATURE ANALYSIS: Theory and operation of LFSR, LFSR as Signature analyzer, Multiple-input Signature Register.

DESIGN FOR TESTABILITY FOR SEQUENTIAL CIRCUITS: Controllability and observability by means of scan register, Storage cells for scan design, classic scan design, Level Sensitive Scan Design (LSSD).

UNIT VI

BUILT IN SELF TEST: BIST concepts, Test pattern generation for BIST exhaustive testing, pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture.

TEXT BOOKS:

1. Parag K. Lala – "Fault Tolerant & Fault Testable Hardware Design" (PHI), Paperback edition, 2002.
2. M. Abramovili, M.A. Breues, A. D. Friedman – "Digital Systems Testing and Testable Design" Jaico Publications, An imprint of W.H.Freeman and company in 1990.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem(DSCE) T 4 C 4

(D0617152) SYSTEMS PROGRAMMING

UNIT I

LANGUAGE PROCESSORS: Introduction, Language Processing Activities, Fundamentals of Language Processing, Fundamental of Language Specifications, Language Processors Development Tools.

UNIT II

DATA STRUCTURES FOR LANGUAGE PROCESSING: Search Data Structures, Allocation Data Structures.

UNIT III

SCANNING ANG PARSING

SCANNING: Introduction, Finite State Automata, regular Expressions, Building DFA's, Performing Semantic Actions, Writing a Scanner.

PARSING: Introduction, Parse Trees and Abstract Syntax Trees, Top Down Parsing and its Algorithm, Predictions and Backtracking, Implementing Top Down Parsing, Comments on Top Down Parsing, Top Down Parsing Without Back Tracking, Practical Top Down Parsing, Bottom Up Parsing and its Algorithm, Simple Precedence, Simple Precedence grammar, Operator Precedence Grammars, Operator Precedence Parsing, Algorithms, LALR Parsing.

UNIT IV

ASSEMBLERS: Elements of Assembly Language Programming, A Simple Assembly Scheme, Pass Structure of Assemblers, A single Pass Assembler for IBM PC.

UNIT V

MACROS AND MACRO PROCESSORS: Macro Definition and Call, Macro Expansion, Nested Macro Calls, Advanced Macro Facilities, Design of Macro Processors.

UNIT VI

COMPILERS AND INTERPRETERS: Aspects of Compilation, Memory Allocation, Compilation of Expressions, Compilation of Control Structures, Code Optimization, Interpreters.

UNIT VII

LINKERS: Relocation and Linking Concepts, Design of Linkers, Self Relocation Programs, A Linker for MS DOS, Linking for Overlays, Loaders.

UNIT VIII

SOFTWARE TOOLS: Software Tools for Program Development, Editors, Debug Monitors, Programming Environments, User Interfaces.

TEXT BOOKS:

1. Systems Programming and Operating Systems by D.M.Dhamdhere, 2nd edition, TMH.
2. System software-An Introduction to systems programming by Leland Beck, 3rd edition, Pearson education, 2011.

REFERENCES:

1. Systems Programming by John J. Donovan, Mc. Graw Hill International Editions.
2. Modern compiler design by David Gallvs, 2nd edition, Addison Willey.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem (DSCE) T 4 C 4

(D0618152) EMBEDDED 'C'

(ELECTIVE-III)

(Common to DSCE & ES)

UNIT I

PROGRAMMING EMBEDDED SYSTEMS IN C: Introduction to embedded system, Processor used, programming language used, operating system used, developing embedded software.

INTRODUCING THE 8051 MICROCONTROLLER FAMILY: Introduction, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption.

UNIT II

EMBEDDED WORLD: Introduction Installing the Keil software and loading the project, Configuring the simulator, Building the target, Running the simulation, Dissecting the program, Building the hardware.

UNIT III

READING SWITCHES: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version),The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code).

UNIT IV

ADDING STRUCTURE TO YOUR CODE: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example.

UNIT V

MEETING REAL-TIME CONSTRAINTS: Introduction, Creating 'hardware delays' using Timer 0 and Timer, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, The need for 'timeout' mechanisms, Creating loop timeouts.

UNIT VI

CREATING AN EMBEDDED OPERATING SYSTEM: Introduction, The basis of a simple embedded OS, Introducing sEOS, Using Timer 0 or Timer 1, alternative architectures, important design considerations when using sEOS.

MULTI-STATE SYSTEMS AND FUNCTION SEQUENCES: Introduction, Implementing a Multi-State (Timed) system, traffic light sequencing, Animatronics dinosaur, implementing a Multi-State (Input/Timed) system, Controller for a washing machine

TEXT BOOKS:

1. Embedded C By Micheal J. Pont Pearson Education, 2002.
2. Embedded C Coding standard-Michael Barr from Neutrino.

REFERENCES:

1. Real Time Concepts for Embedded systems-Qing Li,Caroline Yao, CMP Books 2003.
2. Embedded/Real Time Syatems-KVKK Prasad,Dreamtech press,2005.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem (DSCE) T 4 C 4

(D0619152) WIRELESS SENSOR NETWORKS

(ELECTIVE-III)

UNIT-I

OVERVIEW OF WIRELESS SENSOR NETWORKS: Challenges for Wireless Sensor Networks Characteristics requirements-required mechanisms, Difference between mobile ad-hoc and sensor networks, Applications of sensor networks- Enabling Technologies for Wireless Sensor Networks.

UNIT-II

ARCHITECTURES: Single-Node Architecture - Hardware Components, Energy Consumption of Sensor Nodes , Operating Systems and Execution Environments, Network Architecture - Sensor Network Scenarios, Optimization Goals and Figures of Merit, Gateway Concepts.

UNIT-III

NETWORKING OF SENSORS: Physical Layer and Transceiver Design Considerations, MAC Protocols for Wireless Sensor Networks, Low Duty Cycle Protocols and Wakeup Concepts - S-MAC, the Mediation Device Protocol, Wakeup Radio Concepts, Address and Name Management, Assignment of MAC Addresses, Routing Protocols- Energy-Efficient Routing, Geographic Routing.

UNIT-IV

INFRASTRUCTURE ESTABLISHMENT: Topology Control, Clustering, Time Synchronization, Localization and Positioning, Sensor Tasking and Control.

UNIT-V

SENSOR NETWORK PLATFORMS AND TOOLS: Operating Systems for Wireless Sensor Networks, Sensor Node Hardware – Berkeley Motes, Programming Challenges, Node-level software platforms, Nodelevel Simulators, State-centric programming.

UNIT-VI

APPLICATIONS OF WIRELESS SENSOR NETWORKS: Home automation environmental monitoring, industrial monitoring and control, military for intelligence and communication, structural health monitoring.

TEXTBOOKS:

1. “Protocols and Architectures for Wireless Sensor Networks”, Holger Karl & Andreas Willig, John Wiley, 2005.
2. “Wireless Sensor Networks- An Information Processing Approach", Feng Zhao & Leonidas J. Guibas, Elsevier, 2007.
3. “Wireless Sensor Networks-Technology, Protocols, and Applications”, KazemSohraby, Daniel Minoli, &TaiebZnati, John Wiley, 2007.

REFERENCES:

1. “Wireless Sensor Network Designs”, Anna Hac, John Wiley, 2003.
2. “Networking Wireless Sensors”, BhaskarKrishnamachariCambridge Press, 2005.
3. “Handbook of Sensor Networks: Compact Wireless and Wired Sensing Systems”, Mohammad Ilyas and ImadMahgaob CRC Press, 2005.
4. “Introduction to Data Communication and Networking”, Wayne Tomasi, Pearson Education, 2007.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem (DSCE) T 4 C 4

(D0620152) NETWORK SECURITY AND CRYPTOGRAPHY

(ELECTIVE-III)

(Common to DSCE & ES)

OBJECTIVES:

1. To study various aspects of Network Security Attacks, Services and Mechanisms.
2. To understand the mathematical concepts of various Encryption, Authentication and Digital Signature Algorithms.
3. To standby the design of different general purpose and application specific security Protocols and standards.
4. To identify suitable points for applying security features for network traffic

OUTCOMES:

1. The students will be able to understand and implement various public and private key cryptographic algorithms.
2. The student will be able to protect the system and network from various attacks.
3. The student will be able to design new security approach

UNIT-I

INTRODUCTION: Computer Security Concepts, The OSI Security Architecture, Security Services, Mechanisms, Attacks, Network Security Model, Classical Encryption Techniques – Symmetric Cipher Model, Substitution Techniques, Transposition Techniques, Rotor Machines, Steganography.

BLOCK CIPHERS AND DATA ENCRYPTION STANDARD: Block Cipher Principles, Stream Ciphers and Block Ciphers, Feistel Cipher Structure , Data Encryption Standard, DES Example, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles, AES..

UNIT II

PUBLIC-KEY CRYPTOSYSTEMS: Principles Of Public-Key Cryptosystems, RSA Algorithm, Diffie-Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography, PRNG Based on RSA, PRNG Based on Elliptic Curve Cryptography.

UNIT III

CRYPTOGRAPHIC HASH FUNCTIONS:Applications of Cryptographic Hash functions, Requirements and security, Hash functions based on Cipher Block Chaining, Secure Hash Algorithm (SHA-1), Message authentication Requirements.

MESSAGE AUTHENTICATION CODES: Message authentication functions, Requirements for Message authentication codes, security of MACs, HMAC, MACs based on Block Ciphers, Authenticated Encryption.

UNIT IV

DIGITAL SIGNATURES:Digital Signatures, Digital Signatures Properties, Attacks and Forgeries, Digital Signature Requirements, Direct Digital Signature, Digital Signature Standard, DSS Approach, Digital Signature Algorithm.

KEY MANAGEMENT AND DISTRIBUTION: Symmetric key distribution using Symmetric Encryption, Symmetric key distribution using Asymmetric, Distribution of Public keys, X.509 Certificates, Public key Infrastructure.

UNIT V

USER AUTHENTICATION: Remote user Authentication Principles, Remote user Authentication using Symmetric Encryption, Kerberos, Remote user Authentication using Asymmetric Encryption, Federated Identity Management

ELECTRONIC MAIL SECURITY: Pretty Good Privacy (PGP), S/MIME

UNIT VI

SECURITY AT THE TRANSPORT LAYER (SSL AND TLS) : SSL Architecture, Four Protocols, SSL Message Formats, Transport Layer Security, HTTPS, SSH

SECURITY AT THE NETWORK LAYER (IPSEC): Two modes, Two Security Protocols, Security Association, Security Policy, Internet Key Exchange.

SYSTEM SECURITY

Intruders, Intrusion Detection, Password Management, Types of Malicious Software, Viruses, Virus Countermeasures, Worms, Distributed Denial of Service Attacks, Firewalls.

TEXT BOOKS:

1. Cryptography and Network Security: Principals and Practice, William Stallings, Fifth Edition, Pearson Education.
2. Cryptography and Network Security, Behrouz A. Frouzan and DebdeepMukhopadhyay, 2 nd edition, McGraw Hill Education.

REFERENCES:

1. Cryptography and Network Security, William Stallings, PHI, New Delhi, 2nd Edition, 1999
2. Cryptography and Security, C.K. Shymala, N. Harini and Dr. T.R. Padmanabhan, Wiley-India.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem (DSCE) T 4 C 4

(D0621152) SYSTEM MODELING AND SIMULATION

(ELECTIVE-IV/MOOC)

(Common to DSCE & ES)

UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT II

SIMULATION SOFTWARE: Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT III

BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

UNIT IV

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.

EXOGENOUS SIGNALS AND EVENTS: Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation.

UNIT V

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous-Time Markov processes.

UNIT VI

EVENT DRIVEN MODELS: Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple servers.

SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation mythology.

TEXTBOOKS

1. System Modeling & Simulation, An Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFRENCE BOOKS

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem (DSCE) T 4 C 4

(D0622152) STATISTICAL SIGNAL PROCESSING

(ELECTIVE-IV/MOOC)

UNIT I

OPTIMUM LINEAR FILTERS: Representation of stationary random process – Rational power spectra, Filter parameters and autocorrelation sequence. Forward and backward predictors, Reflection coefficients, AR Process and Linear Prediction.Solution of normal equations – Levinson & Durbin Algorithms, Schur Algorithm.Properties of linear prediction error filters.AR Lattice and ARMA Lattice – Ladder filters. FIR and IIR Wiener filtering and prediction

UNIT II

POWER SPECTRUM ESTIMATION: Estimation of Spectra from finite duration observation of a signal.Periodogram.DFT in power spectrum estimation. Non-parametric methods – Bartlett's welch's and Blackman-Turkey methods; Computational requirements and performance characteristics.

UNIT III

Parametric methods – Relation between auto correlation sequence and model parameters. Methods for AR model parameters. Yule – walker, Burg and unconstrained, Least squares methods. Sequential estimation methods.Selection of AR model order; Moving average (MA) and ARMA models.Capon's minimum variance method.Pisarenko's harmonic decomposition method.Eigen structure methods – Music and ESPIRIT.Order selection criteria.

UNIT IV

ARRAY SIGNAL PROCESSING: Array fundamentals – Spatial signals, Signal models, Spatial sampling. Conventional beam forming-Spatial matched filter, Tapered Beam forming.Optimum Beam forming, Eigen Analysis, Interference cancellation, sidelobe canceller. Performance considerations for optimum beam forming.Basic ideas of direction of arrival estimation using a uniform linear array. Maximum likelihood estimate.Pisaxenko's method.MUSIC.

UNIT V

ADAPTIVE FILTERS: Applications of adaptive filters-Prediction, System modeling, Interference cancellation, Channel equalization. Adaptive direct form FIR filters – MMSE extension, LMS algorithm, properties of LMS algorithm, Recursive Least Squares (RLS) algorithm and its properties. Adaptive Lattice – Ladder filters, properties of lattice – Ladder algorithm.

UNIT VI

Introduction.Moments, cumulant and polyspectra.Higher Order Moments (HOM) and LIT systems, HOM's of linear signal methods.Blind deconvolution.Blind equilization algorithm.Conventional estimators for HOS.Parametric method for estimation of HOS – MA, AR & ARMA methods.Ceptra of HOS.Phase and magnitude retrival from the bispectrum.

TEXTBOOKS:

1. John G. Proakis et.al, "Introduction to Digital Signal Processing", PHI, 1997.
2. Simon Haykins, "Array Signal Processing", P.H. Publication 1985.
3. John G. Proakis, Rader, et.al, "Algorithms for Statistical Signal Processing", Pearson Education, Asia Publishers, Indian edition, 2002.

REFERENCES:

1. D.G. Manolakis, Ingle & S.M. Kogon, "Statistical and Adaptive Signal Processing", McGraw Hill, Int. edition, 2000.
2. S. Kay: Modern Spectral Estimation, "Theory & Applications", PH publication, 1st edition, 1987. 5.

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M.Tech, II-Sem(DSCE) T 4 C 4

(D0623152) FPGA ARCHITECTURE & APPLICATIONS

(ELECTIVE-IV/MOOC)

(Common to DSCE & ES)

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, FPGA – Features, Complex Programmable Logic Devices: ALTERA CPLDs and ALTERA FLEX 10k Series CPLD, Speed Performance.

FPGA: Xilinx logic Cell array, CLB,I/O Block Programmable interconnect, Technology Mapping for FPGA: Library based, LUT based, Multiplexer based Technology Mapping.

UNIT II

CASE STUDIES: programming Technologies, Xilinx XC3000, XC4000, Actel FPGAs, Alteras FPGAs, Plus Logic FPGA, AMD FPGA, Quick Logic FPGA, Algotronix FPGA, Cross point solutions FPGA, FPGA Design Flow.

UNIT III

FINITE STATE MACHINES (FSM): Finite State Machine– State Transition Table, State Assignments for FPGAs. Problem of the Initial State Assignment for One Hot Encoding.

REALIZATION OF STATE MACHINE: Derivation of SM Charts. Realization of State Machine Chart, Alternative Realization of State Machine Chart using Microprogramming.Linked State Machines. One–Hot State Machine,

UNIT IV

FSM ARCHITECTURES: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around A Shift Register. Petri nets for State Machines – Basic Concepts, Properties. Extended Petri nets for Parallel Controllers.

UNIT V

SYSTEMS LEVEL DESIGN: One–Hot Design Method. Use of ASMs in One–Hot Design.Application of One–Hot Method. System Level Design: Controller, Data Path and Functional Partition.

UNIT VI

DIGITAL FRONT END DIGITAL DESIGN FOR FPGAS & ASIC: Using Xilinx ISE EDA Tool Guidelines, Case Studies of Parallel Adder Cell, Parallel Adder, Sequential Circuits: Decade Counters, Parallel Multipliers, Parallel Controllers.

TEXT BOOKS:

1. P.K.Chan& S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.
2. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.

REFERENCES:

1. Fundamentals of logic Design, 5/e, Charles H Roth.Jr.
2. S. Brown, R. Francis, J. Rose, Z. Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
3. Engineering Digital Design, 2/e, Richard F Tinder **Unit VI & VII**.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem(DSCE) P C

3 2

(D0624152) EMBEDDED SYSTEMS PROGRAMMING LAB

(Common to DSCE & ES)

Embedded C programming and testing using 8051 advanced development board and KEIL tools.

1. (i) Program to perform arithematic operations.
   (ii) Program to perform sorting of numbers.
2. Program to shift LED's Left and right.
3. Program for DIP switch interface.
4. Program to display message in LCD 8 bit mode.
5. Program to display picture in GLCD 128X64.
6. Program to send data serially through serial port.
7. Program to display I2C RTC(DS1307) to Hyper terminal window.
8. Program to display digital temperature sensor output.
9. Program for 4X4 matrix keyboard with LCD.
10. (i)Program to interface stepper motor.
11. (ii)Program to interface relay.

Embedded C programming and testing using LPC2148 development kit(Real time environment)

1. Program to interface LED and implement Multi-tasking.
2. Program to display RTC-ADC on LCD.
3. Program to display message on GLCD.

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DIGITAL SYSTEMS AND COMPUTER ELECTRONICS

M.Tech, II-Sem(DSCE) P C

3 2

(D0625152) NEURAL NETWORKS USING MATLAB

1. Simulation of Static Network with concurrent inputs
2. Simulation of Dynamic Network with Sequential inputs
3. Simulation of Dynamic Network with concurrent inputs
4. Simulation of 4-input, Single Neuron Static Network with concurrent inputs
5. Simulation of 2-input, Two Neuron Static Network with concurrent inputs
6. Simulation of 4-input, Two Neuron Static Network with concurrent inputs
7. Incremental Training of Static Network using adapt function
8. Incremental Training of Dynamic Network using adapt function
9. Batch Training of Static Network using adapt function
10. Batch Training of Dynamic Network using train function
11. Batch Training of Static Network using train function
12. Simulation of 2-input Single Neuron Perceptron
13. Training of 2-input Single Neuron Perceptron using learnp function
14. Simulation of 4-Concurrent inputs, double neuron Static Perceptron
15. Creating and Training the Perceptron using “Graphical User Interface (GUI)”
16. Creating the Linear Network and it’s Training
17. Creating the Linear Network with delay and it’s Training
18. Creating the Feedforward Networks and their training using Backpropagation Algorithm