RAJEEV GANDHI MEMORIAL

COLLEGE OF ENGINEERING & TECHNOLOGY

AUTONOMOUS

Affiliated to JNTUA -Anantapuramu, Approved by AICTE-New Delhi,
Accredited by NBA-New Delhi, Accredited by NAAC of UGC with A-Grade
NANDYAL-518 501, KURNOOL Dist., A.P.

DEPARTMENT OF
ELECTRONICS AND COMMUNICATION ENGINEERING

EMBEDDED SYSTEMS

ACADEMIC REGULATIONS,
COURSE STRUCTURE AND SYLLABI

APPLICABLE FOR STUDENTS ADMITTED INTO

M.TECH (REGULAR) FROM 2015-16

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

AUTONOMOUS

EMBEDDED SYSTEMS

(Affiliated to J.N.T.U.A, Ananthapuramu)

ACADEMIC REGULATIONS, COURSE STRUCTURE AND DETAILED SYLLABI

M.Tech. (Regular) from 2015-16

For pursuing Two year Master (post graduate) Degree of study in Engineering (M.Tech.), offered by Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal - 518501 under Autonomous status and herein referred to as RGMCET (Autonomous).

All the rules specified herein approved by the Academic Council will be in force and applicable to students admitted from the Academic Year 2015-16 onwards. Any reference to "Institute" or "College" in these rules and regulations shall stand for Rajeev Gandhi Memorial College of Engineering and Technology (Autonomous).

All the rules and regulations, specified hereafter shall be read as a whole for the purpose of interpretation as and when a doubt arises, the interpretation of the Chairman, Academic Council is final. As per the requirements of statutory bodies, the Principal, Rajeev Gandhi Memorial College of Engineering and Technology shall be the Chairman, Academic Council.

Academic Regulations 2015 for M.Tech. (Regular)
(Effective for the students admitted into first year from the Academic Year 2015-2016)

The M.Tech. Degree of Jawaharlal Nehru Technological University Anantapur, Ananthapuramu shall be conferred on candidates who are admitted to the M.Tech. program at RGMCET, Nandyal and they shall fulfil all the requirements for the award of the Degree.

1.0 Eligibility for Admissions:

Admission to the above program shall be made subject to the eligibility, qualifications and specialization prescribed by Andhra Pradesh State Council of Higher Education (APSCHE) from time to time.

Admissions shall be made on the basis of merit rank obtained in GATE examination or PGCET conducted by any University of Andhra Pradesh designated by Govt. of A. P., or on the basis of any other order of merit prescribed by APSCHE, subject to the reservations prescribed by the Government of A. P. from time to time.

2.0 Award of M.Tech. Degree:

2.1 The student shall be declared eligible for the award of the M.Tech. degree, if he/she pursues a course of study and completes it successfully for not less than prescribed course work duration and not more than double the prescribed course work duration.

2.2 The student, who fails to fulfil all the academic requirements for the award of the degree within double the course work duration from the year of his admission, shall forfeit his seat in M.Tech. course.

2.3 The minimum clear instruction days for each semester shall be 95.

3.0 Courses of Study:

The following specializations are offered at present for the M.Tech. course of study.

1. Computer Science (CSE)
2. Digital Systems and Computer Electronics (ECE)
3. Embedded Systems (ECE)

4. Machine Design (Mechanical Engineering)
5. Power Electronics (EEE)
6. Software Engineering (IT)
7. Structural Engineering (CE)

and any other course as approved by the appropriate authorities from time to time.

4.0 Course pattern:

4.1 The entire course of study is of four semesters. During the first and second semesters the student has to undergo course work and during the third and fourth semesters the student has to carry out project work.

4.2 The student shall be eligible to appear for the End Examination in a subject, but absent at it or has failed in the End Examination may appear for that subject at the supplementary examination.

Table 1: Credits

Subject	Semester			
	Periods /Week	Credits	Internal marks	External marks
Theory	04	04	40 (25 Internal Test+15 Assignment)	70
Practical	03	02	50	50
Seminar		02	100	
Comprehensive Viva – voce 1		02		50
Comprehensive Viva - voce 2		02		50
Project		12		

Table2: Course pattern

Semester	No.of Subjects	Number of Labs	Total credits	
First	04-Subjects 01-Elective 01-MOOC/Elective	 02 Comprehensive Viva 1	04X4=16 01X4=04 01X4=04 02X2=04 01X2=02	30
Second	04-Subjects 01-Elective 01-MOOC/Elective	 02 Comprehensive Viva 2	04X4=16 01X4=04 01X4=04 02X2=04 01X2=02	30
Third	Seminar(3rd semester) Intermediate Evaluation of Project work(3rd semester)			02 04
Fourth	Project Work			08
			Total credits	**74**

5.0 Attendance:

5.1 The candidate shall be deemed to have eligibility to write end semester examinations, if he has secured a minimum of 75% of attendance in aggregate of all the subjects.

5.2 Condonation of shortage of attendance up to 10%, i. e. 65% and above and below 75% may be given by the College academic committee consisting of Principal, Head of the Department and a senior faculty member.

5.3 Condonation of shortage of attendance shall be granted only on genuine and valid reasons on representation by the candidate with supporting evidence.

5.4 Shortage of attendance below 65% shall in no case be condoned.

5.5 The candidate shall not be promoted to the next semester unless he fulfils the attendance requirements of the previous semester.

5.6 Attendance in each subject will be recorded in the marks memo.

5.7 The attendance in each subject will be recorded in the Marks memo.

6.0 Evaluation:

6.1 For theory subjects the distribution shall be 40 marks for Internal Evaluation (25 marks for Internal test and 15 marks for assignments/ field work) and 60 marks for the End-Examination.

6.2 Each Internal Test question paper shall contain 5 questions, of which the First question is compulsory and three questions are to be answered from the remaining four. Compulsory question carries 10 marks (It contains 5 short answer questions). The remaining 3 questions carry 5 marks each. Each question shall have a,b,c.... parts. The duration of internal test will be for 2 hours. First test to be conducted in 3 units in the middle of the semester and second test to be conducted in the remaining 3 units of each subject at end the semester. There shall be two assignments in each subject (problem based/ field work) for the award of 15 marks so that internal component (marks) will be 40 marks (25 marks for internal test+15 marks for assignments / field work). For awarding of 25 Internal marks the performance of the student in two internal examinations conducted will be considered by giving a weightage of 0.75 for the better score and 0.25 for the other score.

6.3 The End Examination question paper will have 7 questions and students have to answer 5 questions. However, the first question is compulsory and it consists of 6 short answer questions, each carrying 2 marks. The next 4 questions are to be answered from the remaining 6 questions and each carries 12 marks. Each 12 marks question shall have a, b, c .. parts.

6.4 Elective subjects will commence from 1st semester. Out of the electives offered in 1st / 2nd semester, one elective will be MOOC / Electives offered by the department. Any student who is interested can opt for the MOOC/ Electives offered by the department and acquire the required credits. Even if the student opts MOOC, he has to write two internal tests besides the end examination conducted by the institute like other subjects. However, he has to obtain the certificate from the organization in which he has registered. Any MOOC selected

by the student should be of more than 45 hours duration and also from the reputed organization. Attendance of the student who has opted for MOOC will be taken from the remaining subjects and labs only in that semester while finalizing the attendance for fulfilling the minimum requirements of attendance for promotion to next semester. Attendance will not be recorded for MOOC. Where ever MOOC is opted by the student, the evaluation procedure will be similar to any subject offered by the department.

6.5 For practical subjects, 50 marks shall be for the End Semester Examinations and 50 marks will be for internal evaluation based on the day-to-day performance.Laboratory examination for M.Tech.. Course shall be conducted with two Examiners, one of them being Laboratory Class Teacher and second Examiner shall be outside from the institute (External examiner).

6.6 Student has to undergo a comprehensive viva pertaining to his specialization which carries 50 marks in each semester. He has to secure 50% marks to obtain required credits.Comprehensive viva will be conducted at the end of 1st and 2nd semester by the committee consisting of HOD, senior faculty member and external Examiner from outside the institute. For this, HOD of the Department shall submit a panel of 4 Examiners, who are eminent in that field. One from the panel will be selected by the principal of the institute as external Examiner for comprehensive viva.

6.7 For Seminar 100 marks shall be for internal evaluation. The candidate has to secure a minimum of 50 marks to be declared successful. The assessment will be made by a board consisting of HOD and two internal experts at the end of 3rd semester.

6.8 The candidate shall be deemed to have secured the minimum academic requirement in a subject if he secures a minimum of 40% of marks in the End Examination and a minimum aggregate of 50% of the total marks in the End Examination and Internal evaluation taken together.

6.9 In case the candidate does not secure the minimum academic requirement in any subject (as specified in 5.0), he has to reappear for the Semester Examination either supplementary or regular in that subject, or repeat the course when next offered or do any other specified subject as may be required.

7.0 Re-registration for improvement of Internal marks:

Following are the conditions to avail the benefit of improvement of internal marks.

7.1 The candidate should have completed the course work and obtained examinations results for 1st& 2nd semesters.

7.2 He should have passed all the subjects for which the internal marks secured are more than 50%.

7.3 Out of the subjects the candidate has failed in the examination due to Internal marks secured being less than 50%, the candidate shall be given one chance for each Theory subject and for a maximum of three Theory subjects for Improvement of Internal marks.

7.4 The candidate has to re-register for the chosen subjects and fulfil the academic requirements as and when they are offered.

7.5 For each subject, the candidate has to pay a fee equivalent to one tenth of the semester tuition fee and the amount is to be remitted in the form of D. D. in favour of the Principal, RGMCET payable at RGMCET, Nandyal branch along with the requisition through the HOD of the respective Department.

7.6 In case of availing the Improvement of Internal marks, the internal marks as well as the End Examinations marks secured in the previous attempt (s) for the re-registered subjects stand cancelled.

8.0 Evaluation of Project / Dissertation work :

Every candidate shall be required to submit thesis or dissertation after taking up a topic approved by the Department.

8.1 Registration of Project work: The candidate is permitted to register for the project work after satisfying the attendance requirement of all the courses (theory and practical courses of 1st& 2nd Sem)

8.2 An Internal Department Committee (I.D.C.) consisting of HOD, Supervisor and One Internal senior expert shall monitor the progress of the project work.

8.3 The work on the project shall be initiated in the penultimate semester and continued in the final semester. The duration of the project is for two semesters. The candidate can submit Project thesis with the approval of I.D.C. after 36 weeks from the date of registration at the earliest. Extension of time within the total permissible limit for completing the programme is to be obtained from the Head of the Institution.

8.4 The student must submit status report at least in three different phases during the project work period. These reports must be approved by the I.D.C. before submission of the Project Report.

8.5 The candidate shall be allowed to submit the thesis/dissertation only after passing in all the prescribed subjects (both theory and practical) and then take viva voce examination of the project. The viva - voce examination may be conducted once in two months for all the candidates submitted during that period.

8.6 Three copies of the Thesis/Dissertation certified in the prescribed form by the supervisor & HOD shall be submitted to the institute.

8.7 The Department shall submit a panel of 4 experts for a maximum of 4 students at a time. However, the thesis/dissertation will be adjudicated by the board consists of HOD, concerned supervisor and one external Examiner from other institute nominated by the principal from a panel of Examiners submitted by the Department HOD to the Controller of Examinations.

8.8 If the report of the board is favourable in viva voce examination, the board shall jointly report candidates work as:

1. Good
2. Satisfactory
3. Not satisfactory

If the report of the viva voce is not satisfactory the candidate will retake the viva voce examination after three months. If he fails to get a satisfactory report at the second viva voce examination he will not be eligible for the award of the degree unless the candidate is permitted to revise and resubmit the thesis.

9.0 Award of Degree and Class:

After the student has satisfied the requirements prescribed for the completion of the program and is eligible for the award of M. Tech. Degree he shall be placed in one of the following classes:

Table 3: Award of division

Class Awarded	**% of marks to be secured**	Division/ Class	CGPA	From the aggregate marks secured from the 74 Credits.
First Class with Distinction	70% and above	First Class With Distinction	≥ 7.5	
First Class	Below 70% but not less than 60%	First Class	6.5 *and* < 7.5	
Second Class	Below 60% but not less than 50%	Second Class	≥ 5.5 *and* < 6.5	

(The marks in internal evaluation and End Examination shall be shown separately in the marks memorandum)

10.0 *Grading:*

After each subject is evaluated for 100 marks, the marks obtained in each subject will be converted to a corresponding letter grade as given below, depending on the range in which the marks obtained by the student falls.

Table 4: Conversion into Grades and Grade points assigned

Range in which the % of marks in the subject fall	Grade	Grade point Assigned	Performance
90 to 100	O	10	Outstanding
80 to 89.9	A^+	09	Excellent
70 to 79.9	A	08	Very good
60 to 69.9	B^+	07	good
50 to 59.9	B	06	Pass
<50	F	00	Fail
Ab	AB	00	Fail

10.1 Requirement for clearing any subject: The students have to obtain a minimum of 40% in End Examination and they have to score minimum of 50% marks from Internal and external exam marks put together to clear the subject. Otherwise they will be awarded fail grade.

10.2 F is considered as a fail grade indicating that the student has to reappear for the end supplementary examination in that subject and obtain a non fail grade for clearing that subject.

10.3 To become eligible for the award of degree the student must obtain a minimum CGPA of 6.0.

11.0 Supplementary Examinations:

Apart from the regular End Examinations the institute may also schedule and conduct supplementary examinations for all subjects for the benefit of students with backlogs. Such students writing supplementary examinations as supplementary candidates may have to write more than one examination per day. The student is not permitted to improve his performance in any subject in which he has obtained pass grade.

12.0 *Grade Point Average (GPA) and Cumulative Grade Point Average(CGPA)*

The Grade Point Average (GPA) for each semester and Cumulative Grade Point Average (CGPA) up to any semester are calculated as follows:

i) Semester Grade Point Average will be computed as follows:

$$GPA = \frac{\sum_1^n C_i \times GP_i}{\sum_1^n C_i}$$

Where, n is the number of subjects in that semester. C_i is Credits for the subjects. GP_i is the grade point obtained for the subject and the summation is over all the subjects in that semester.

ii) A Cumulative Grade Point Average (CGPA) will be computed for

every student at the end of each semester. The CGPA would give the cumulative performance of The student from the first semester up to the end of the semester to which it refers and is calculated as follows

$$CGPA = \frac{\sum_1^m GPA_j \times TC_i}{\sum_1^m TC_j}$$

Where 'm' is the number of semester under consideration. TC_j the total number of credits for a j^{th} semester and GPA_j is the Grade Point Average of the j^{th} semester. Both GPA and CGPA will be rounded off to the second digit after decimal and recorded as such.

While computing the GPA / CGPA the subjects in which the student is awarded zero grade points will also be included.

13.0 Grade Sheet:

A grade sheet (Memorandum) will be issued to each student indicating his performance in all subjects of that semester in the form of grades and also indicating the GPA and CGPA.

14.0 Transcripts:

After successful completion of prerequisite credits for the award of degree a Transcript containing performance of all academic years will be issued as a final record. Duplicate transcripts will also be issued if required after the payment of requisite fee and also as per norms in vogue.

15.0 Minimum Instruction Days:

The minimum instruction days for each semestershall be 95 clear instruction days excluding the days allotted for tests/examinations and preparation holidays declared if any.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

AUTONOMOUS

EMBEDDED SYSTEMS

16.0 Amendment of Regulations:

The college may, from time to time, revise, amend or change the regulations, scheme of examinations and syllabi. However the academic regulations of any student will be same throughout the course of study in which the student has been admitted.

17.0 Transfers

There shall be no branch transfers after the completion of admission process.

18.0 Withholding of results:

If the candidate has not paid any dues to the institute or if any case of in-discipline is pending against him, the result of the candidate will be withheld and he will not be allowed for the next semester. The issue of the degree is liable to be withheld in such cases.

19.0 Transitory Regulations:

Candidates who have discontinued or have been detained for want of attendance are eligible for admission to the same or equivalent subjects as and when subjects are offered, subject to 2.0 and 5.0.

20.0 Rules of Discipline:

20.1 Any attempt by any student to influence the teachers, Examiners, faculty and staff of Examination section for undue favours in the exams, and bribing them either for marks or attendance will be treated as malpractice cases and the student can be debarred from the college.

20.2 When the student absents himself, he is treated as to have appeared and obtained zero marks in that subject (s) and grading is done accordingly.

20.3 When the performance of the student in any subject (s) is cancelled as a punishment for indiscipline, he is awarded zero marks in that subject (s).

20.4 When the student's answer book is confiscated for any kind of attempted or suspected malpractice, the decision of the Chief Superintendent is final.

21.0 General:

21.1 The Academic Regulations should be read as a whole for the purpose of any interpretation.

21.2 In the case of any doubt or ambiguity in the interpretation of the above rules, the decision of the College Academic Council is final.

21.3 The Institute may change or amend the academic regulations or syllabi at any time and the changes or amendments made shall be applicable to all the students with effect from the dates notified by the Institute.

21.4 *Where the w*ords "he", "him", "his", occur in the regulations, they include "she", "her", "hers".

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

AUTONOMOUS

EMBEDDED SYSTEMS

COURSE STRUCTURE

M.TECH, I-SEMESTER

Code	Subject	Scheme of instruction periods/week		Credits	Scheme of Examination		
		Theory	Practical		Internal	External	Total
D0602151	Embedded System Concepts	4	-	4	40	60	100
D0603151	Advanced Computer Architecture	4	-	4	40	60	100
D5501151	Advanced DSP and Applications	4	-	4	40	60	100
D5502151	Micro Controllers & Interfacing	4	-	4	40	60	100
	ELECTIVE-I	4	-	4	40	60	100
D5503151	Principles of Operating Systems						
D5504151	*Radio Frequency Identification*						
D5505151	Advanced Computer Networks						
	ELECTIVE-II/MOOC	4	-	4	40	60	100
D0608151	Expert Systems						
D0609151	VLSI Technology						
D0610151	Algorithms for VLSI Design Automation						
D5506151	Micro Controllers and Interfacing Lab	-	3	2	50	50	100
D0611151	FPGA/CPLD Lab	-	3	2	50	50	100
D5507151	Comprehensive Viva-I	-	-	2	-	50	50
	Total	24	6	30	340	510	850

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

AUTONOMOUS

EMBEDDED SYSTEMS

COURSE STRUCTURE

M.TECH, II-SEMESTER

Code	Subject	Scheme of instruction periods/week		Credits	Scheme of Examination		
		Theory	Practical		Internal	External	Total
D5508152	Embedded System Design	4	-	4	40	60	100
D5509152	Real Time Operating Systems	4	-	4	40	60	100
D5510152	Hardware Software Co-design	4	-	4	40	60	100
D0618152	Embedded 'C'	4	-	4	40	60	100
	ELECTIVE-III	4	-	4	40	60	100
D5511152	CMOS Digital IC Design						
D0620152	Network Security and Cryptography						
D5512152	Analog IC design						
	ELECTIVE-IV/MOOC	4	-	4	40	60	100
D0621152	System Modeling and Simulation						
D5513152	Low Power VLSI Design						
D0623152	FPGA Architecture & Applications						
D0624152	Embedded Systems Programming Lab	-	3	2	50	50	100
D5514152	CMOS Digital IC Design Lab	-	3	2	50	50	100
D5515152	Comprehensive Viva-II	-	-	2	-	50	50
	Total	24	6	30	340	510	850

M.TECH, III-SEMESTER & IV-SEMESTER

Code	Subject	Credits	Internal Marks	External Marks	Total
D5516153	Seminar (End of III Semester)	2	100	-	100
D5517153	Project work	12	-	-	-

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech I-Sem (ES) T C
4 4

(D0602151) EMBEDDED SYSTEM CONCEPTS

(Common to DSCE & ES)

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems.

UNIT II

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems: I^2C bus, CAN bus. Communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT III

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space.

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique.

UNIT IV

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes.

UNIT V

INSTRUCTION SETS: Introduction, preliminaries, ARM processor: Processor and Memory organization, data operations, flow of control, simple examples. SHARC processor: Memory organization, data operations, flow of control, Simple examples

UNIT VI

SYSTEM DESIGN TECHNIQUES: Design methodologies, requirement analysis, specifications: Control-Oriented specification languages, advanced specifications. system analysis and architecture design, quality assurance techniques.

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes, etc.

TEXT BOOKS:

1. Computers as a component: principles of embedded computing system design- wayne wolf, reprint 2009.
2. An embedded software premier: David E. Simon, 2007, 4th edition.
3. Rajkamal, “Embedded systems: Architecture, Programming and Design”, TMH

REFERENCES:

1. Embedded real time systems programming-Sri ram V Iyer, PankajGupta, TMH, 2004.
2. Embedded system design- A unified hardware/software introduction- frank vahid, tony D. Givargis, John Willey, 2002.
3. Embedded/real time systems-KVKK Prasad, Dreamtech press, 2005.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) T 4 C 4

(D0603151) ADVANCED COMPUTER ARCHITECTURE

(Common to DSCE & ES)

UNIT I

FUNDAMENTALS OF COMPUTER DESIGN: Technology trends, cost, price and their trends, cost of an integrated circuits, measuring and reporting performance, quantitative principles of computer design-Amdahl's law, CPU performance equation.

UNITII

INSTRUCTIONSETPRINCIPLESANDEXAMPLES:
classifyinginstructionset,memoryaddressing,typeandsizeofoperands, addressingmodesforsignalprocessing, operationsintheinstructionset-instructionsforcontrolflow-encodingan instructionset.-theroleofcompiler

UNITIII

INSTRUCTIONLEVELPARALLELISM(ILP): Instruction-level parallelism concepts and challenges, Overcomingdatahazards, dynamic scheduling using tomasulo's approach, reducingbranchcosts, highperformanceinstruction delivery, hardwarebasedspeculation,limitation of ILP, ILPSOFTWAREAPPROACH:Basic CompilerTechniques,Static BranchProtection,VLIWApproach,H.WsupportformoreILPat compiletime, conditional or predicated instructions, compiler speculation with hardware support,H.WversesS.Wsolutions

UNIT IV

MEMORY HIERARCHY DESIGN: review of caches, cache performance,reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

MULTIPROCESSORSANDTHREADLEVELPARALLELISM:a taxonomy of parallel architecture, symmetricsharedmemoryarchitectures-basic schemes for enforcing coherence, snooping protocols,distributedsharedmemory, Synchronization,multi-threading.

UNITV

STORAGESYSTEMS: Types of storage devices,Buses-connecting I/O devices to CPU/memory,RAID,errorsandfailures in real systems,bench marks of storage performance and availability,designing a I/O system.

UNITVI

INTERCONNECTIONNETWORKSANDCLUSTERS: Interconnectionnetworkmedia, practicalissuesi ninterconnectingnetworks-connecting the network to the computer, standardization, message failure tolerance, node failure tolerance, examples of interconnection networks,clusters,designing a cluster

TEXTBOOKS:

1. John. Hennessy &DavidA.PattersonMorganKufmann, "ComputerArchitectureAquantitativeapproach", 3rdedition (AnImprintofElsevier), 2003.

REFERENCES:

1. KaiHwangandA. Briggs, "ComputerArchitectureandparallelProcessing", InternationalEditionMcGraw-Hill, 1985.
2. DezsoSima,TerenceFountain,PeterKacsuk, "AdvancedComputerArchitectures", Pearson, 2008.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) T 4 C 4

(D5501151) ADVANCED DSP & APPLICATIONS

UNIT I

LTI DISCRETE-TIME SYSTEMS IN THE TRANSFORM DOMAIN: The frequency response, The transfer function, Types of Linear-Phase transfer functions-Ideal filters, Simple FIR digital filters, Simple IIR digital filters, comb filters, Zero phase and linear phase transfer functions, Types of linear phase FIR transfer functions.Allpass transfer function, Complementary Transfer Functions, Inverse Systems, System identification, Digital Two-Pairs.

UNIT II

DIGITAL FILTER STRUCTURE AND DESIGN: All pass filters, Tunable IIR Digital filter, IIR & FIR tapped Cascaded Lattice Structures, Parallel All pass realization of IIR Transfer Functions, Digital Sine-Cosine generator. Computational Complexity of Digital filter Structures, Design of IIR filter using pade' approximation, Least square design methods, Design of computationally efficient FIR filters.

UNIT III

DSP ALGORITHMS: FFT, Sliding Discrete Fourier transform, DFT Computation Over a narrow Frequency Band, Split Radix FFT, Linear filtering approach to Computation of DFT using Chirp Z-Transform.

UNIT IV

ANALYSIS OF FINITE WORD LENGTH EFFECTS: The Quantization Process and errors, Quantization of fixed-point Numbers, Analysis of Coefficient quantization effects, A/D conversion Noise Analysis, Analysis of Arithmetic Round of errors.

UNIT V

ADAPTIVE FILTERS: FIR adaptive filters - Widrow-Hoff LMS adaptive algorithms and implementation, Adaptive channel equalization - adaptive echo cancellation - Adaptive noise cancellation - Adaptive recursive (IIR) filters – RLS algorithms and its applications( ), Introduction to Kalamaan filter.

UNIT VI

APPLICATIONS OF DIGITAL SIGNAL PROCESSING: Dual Tone Multi-frequency Signal Detection, Spectral Analysis using DFT, Short term discrete Fourier Transform, Musical Sound Processing, Digital FM stereo generation. Discrete time analytic signal generation, Voice privacy system, Sub band coding of speech and audio signals, Trans multiplexers, oversampling A/D Converter, oversampling D/A Converter.

TEXT BOOKS:

1) Digital Signal Processing by Sanjit K Mitra, Tata MCgraw Hill Publications, 1st edition, 1999.
2) Digital Signal Processing Principles, Algorithms,Applications By J G Proakis, D G.Manolokis,PHI, 3rd edition, 2003.
3) Adaptive filter theory by Simon Haykin, Pearson education, 4th edition, 2003.

REFERENCES:

1) Discrete time signal processing by A.V.Oppenhiem, R.W. Schafer, Pearson education Asia, 2nd edition, 1996.
2) Statistical and adaptive signal processing by Dimitris G Manolakis&VinayK.Ingle, McGraw Hill, 2000.
3) Digital Signal Processing by A.V.Oppenhiem and R.W. Schafer, PHI, 1st edition, 2004.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) T 4 C 4

(D5502151) MICROCONTROLLERS & INTERFACING

UNIT I

INTEL 8051: Architecture of 8051, Memory Organization, Register banks, Bit addressing media, SFR area, addressing modes, Instruction set, Programming examples.

UNIT II

INTEL 8051: 8051 Interrupt structure, Timer modules, Serial Features, Port structure, Power saving modes. External Memory Interfacing.

UNIT III

MOTOROLA 68HC11: Controllers features, Different modes of operation and memory map, Functions of I/O ports in single chip and expanded multiplexed mode, External Memory Interfacing.

UNIT IV

MOTOROLA 68HC11: Timer system, Input capture, Output compare and pulsed accumulator features of 68HC11, Serial peripherals, Serial Communication interface, Analog to digital conversion features.

UNIT V

PIC MICROCONTROLLERS: Program memory, CPU registers, Register file structure, Block diagram of PIC 16C74, I/O ports. Timer 0,1 and 2 features, Interrupt logic, serial peripheral interface, PIC family parts.

UNIT VI

Applications of Microcontrollers: Design of Embedded Systems using the micro controller 8051 for applications in the area of Communications, Automotives, industrial control.

TEXT BOOKS:

1) M.A. Mazadi, J.G. Mazidi&RolinD.McKinlay "The 8051 Micro Controller & Embedded Systems using assembly and C", Pearson Education. Asia, 2nd edition, 2006.
2) John B. Peatman, Designing with PIC Micro Controllers, Low price edition, Pearson Education, 7th reprint 2004.
3) Jonathan W. Valvano, Embedded Microcomputer systems, Real Time Interfacing, Brookes/Cole, Thomas learning, 2nd edition 2007.
4) Raj Kamal "Microcontrollers: Architecture, Programming, Interfacing and System Design" Pearson Education India, 2009

REFERENCES:

1) 8-bit Embedded Controllers, INTEL Corporation 1990.
2) Motorola 68HC11 data sheets.
3) PIC 16C74 data sheets.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) T C
4 4

(D5503151) PRINCIPLES OF OPERATING SYSTEMS

(ELECTIVE-I)

UNIT I

INTRODUCTION: Operating system definition, Objective and functions, types, different parts, Structure of operating system, trends- parallel computing, distributed computing; Open systems, Hardware, software, firmware.

UNIT II

PROCESS SCHEDULING: Definition of a process; process states, transitions, process control, suspend and process, interrupt processing, nucleus of an operating system; parallel processing; Mutual exclusion, Critical Section; Solution of mutual exclusion; Semaphores; Deadlock- occurrence, prevention, detection and recovery.

UNIT III

STORAGE MANAGEMENT: Storage organization, management strategies, hierarchy; virtual storage, paging, segmentation.

FILE SYSTEM MANAGEMENT**:** File system (function of a file system)- data hierarchy, blocking and buffering, file organization, queued and basic access methods, backup and recovery.

UNIT IV

I/O MANAGEMENT: (functions of I/O management subsystem), Distributed computing- OSI view, OSI network management, MAP, TOP, GOSIP, TCP/IP.

UNIT V

OS SECURITY: Requirements, external security, operational security, surveillance, threat monitoring; Introduction to Cryptography.

UNIT VI

CASE STUDIES: UNIX- Shell, Kernel, File System, Process Management, Memory Management, I/O System, Distributed UNIX. Example of operating system-MS-DOS, Windows, OS/2, Apple Macintosh & Linux.

TEXT BOOKS:

1) Dietal H.M“An Introduction to OS” Pearson Education Pvt.Ltd/PHI New Delhi, 12th Indian Reprint 2003.
2) SilberschatzA, Galvin. P and Gagne.G, “Operating System Concepts”,John Wiley and Sons. Singapore,2002.

REFERENCES:

1) William Stallings, “Operating Systems”, Pearson Education Pvt.Ltd.
2) D.M. Dhamdhere, “Operating Systems – A Concept Approach”, Tata McGraw Hill, 2003.
3) Andrew S.Tanenbaum, “Modern OS”PHI Pearson Education Pvt. Ltd New Delhi, 3rd Indian Reprint 2004.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) T 4 C 4

(D5504151) RADIO FREQUENCY IDENTIFICATION

(ELECTIVE-I)

UNIT I

UNDERSTANDING RFID TECHNOLOGY: Introduction, RFID Technology, The Elements of an RFID system, Coupling, Range, and Penetration, RFID Applications, VeriChip and Mark of the Beast.

UNIT II

A HISTORY OF THE EPC: Introduction, The Distributed Intelligent Systems Center, Meanwhile, at Procter & Gamble, "Low-Cost" RFID Protocols, "Low-cost" Manufacturing, The Software and the Network, Privacy, Harnessing the Juggernaut, The Six Auto-ID Labs, The Evolution of the Industry, The Creation of EPC global.

UNIT III

RFID AND GLOBAL PRIVACY POLICY: Introduction, Definitions of Privacy, Definitions of Personal Information, History of Current Privacy Paradigm, Mapping the RFID Discovery process, Functions and Responsibilities for chips, Readers, and Owners, Privacy as a Fundamental Human Right, Constitutional Rights.

UNIT IV

PRIVACY OF RFID, AND REGULATION: Introduction, Understanding RFID's Privacy Threats. RFID and the United States Regulatory Landscape

UNIT V

REGULATION OF RFID:

Introduction, Current State of RFID Policy, Individuals, Business, Government, Miscellaneous, Integrity and Security of the System, Government Access, Health Impact, Labor Impact

UNIT VI

APPLICATIONS: RFID Payments at ExxonMobil, Exxon Mobil Corporation, Transforming the Battlefield with RFID, Logistics and the Military, RFID in the Pharmacy, CVS and Auto-ID, Project Jump Start, RFID in the Store.

TEXT BOOKS:

1. Simson Garfinkel and Beth Rosenberg, "RFID Applications, Security, and privacy", Pearson Education
2. Steven Shepard, "Radio Frequency Identification", First edition, McGraw-Hill Professional.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) T 4 C 4

(D5505151) ADVANCED COMPUTER NETWORKS

(ELECTIVE-I)

UNIT I

CONGESTION AND QUALITY OF SERVICE (QOS)Data traffic, Congestion, Congestion Control, Open loop and Closed Loop Congestion Control in TCP and Frame Relay, Quality of Service, Flow Characterization, Flow Classes, Need For QoS, Resource Allocation, Best Effort Service Features, Techniques to Improve QoS.

UNIT II

QUEUE MANAGEMENT:Passive, Active (RED), and Fair (BRED, Choke) Queue Management Schemes, Scheduling, Traffic Shaping, Resource Reservation and Admission Control Scheduling, Integrated and Differential Services.

UNIT III

WIRELESS LOCAL AREA NETWORKS:Introduction, Wireless LAN Topologies, Wireless LAN Requirements, the Physical Layer, the Medium Access Control (MAC) Layer, Latest Developments. Wireless Personal Area Networks (WPANs):Introduction to PAN Technology and Applications, Commercial Alternatives- Bluetooth, Home RF. Wireless Wide Area Networks and MANS:The Cellular Concept, Cellular Architecture, The First- Generation Cellular Systems, The Second- Generation Cellular Systems, The Third- Generation Cellular Systems, Wireless in Local Loop, Wireless ATM, IEEE 802.16 Standard.

UNIT IV

CELLULAR SYSTEMS AND INFRASTRUCTURE - BASED WIRELESS NETWORKS:Cellular Systems Fundamentals, Channel Reuse, SIR and User Capacity, Interference Reduction Techniques, Dynamic Resource Allocation, Fundamental Rate Limits. Virtual Private Network (VPN):Types of VPN, VPN General Architecture, Current VPN Advantages and Disadvantages, VPN Security Issues, VPN Standards.

UNIT V:

ATM PROTOCOL REFERENCE MODEL:Introduction, Transmission Convergence (TC) Sub-layer, Physical Medium Dependent (PMD) Sub-layer, Physical Layer Standards for ATM. ATM Layer:ATM Cell Header Structure at UNI, ATM Cell Header Structure at NNI, ATM Layer Functions. ATM Adaptation Layer:Service Classes and ATM Adaptation Layer, ATM Adaptation Layer 1 (AAL1), ATM Adaptation Layer 2 (AAL2), ATM Adaptation Layer 3/4 (AAL3/4), ATM Adaptation Layer 5 (AAL5). ATM Traffic and Service Parameterization:ATM Traffic Parameters, ATM Service Parameters, Factors Affecting QoS Parameters, ATM Service Categories, QoS and QoS Classes.

UNIT VI

INTERCONNECTION NETWORKS:Introduction, Banyan Networks- Properties, Crossbar Switch, Three Stage Class Networks, Rearrangeable Networks, Folding Algorithm, Benes Networks, Looping Algorithm, Bit- Allocation Algorithm. SONET/SDH:SONET/SDH Architecture, SONET Layers, SONET Frames, STS Multiplexing, SONET Networks.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

TEXTBOOKS

1. "Wireless Communications"by Andrea Goldsmith, 2005, Cambridge University Press.
2. "Ad Hoc Wireless Networks: Architectures and Protocols"by C. Siva Ram Murthy and B.S.Manoj, 2004, PHI.
3. "Data Communication and Networking**"** by B. A.Forouzan, 2nd updating, 2004,TMH

REFERENCES

1. "Introduction to Broadband Communication Systems" bySadiku, Mathew N.O., Akujuobi, Cajetan.M, PHI
2. "Wireless Networks" by P. Nicopolitidis ,A. S. Pomportsis, G. I. Papadimitriou, M. S. Obaidat, 2003, JohnWiley & Sons
3. "High Performance TCP / IP Networking**"** by Mahaboob Hassan, Jain Raj, PHI

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) T C
4 4

(D0608151) EXPERT SYSTEMS

(ELECTIVE – II/MOOC)
(Common to DSCE & ES)

UNIT I

KNOWLEDGE REPRESENTATION AND ISSUES: Notational systems: Trees, graphs, hierarchies, propositional and predicate logics, frames, semantics networks, constraints, conceptual dependencies, database, knowledge discovery in databases (KDD).

UNIT II

SEARCH: State-space representations, Depth-first, breadth-first, heuristic search, Planning and game playing, Genetic algorithms.

UNIT III

LOGICAL REASONING AND PROBABILISTIC REASONING: Predicate, Calculus resolution, completeness, and strategies, Unification, Prolog, monotonic and non-monotonic reasoning.

UNIT IV

EXPERT SYSTEMS: Probabilistic inference networks, Fuzzy inference rules, Bayesian rules. Dumpster - Shafer Calculus.Expert Systems, Organization, tools, limits, examples.

UNIT V

LEARNING AND COMMON SENSANE REASONING: Robot actions, strips, triangle tables, case based reasoning, spatial and temporal formalisms.

UNIT VI

Knowledge acquisition, classification rules, self-directed systems.

NEURAL NETWORKS: Principles, biological analogies, Training (techniques and errors), Recognition.

TEXT BOOKS:

1. Charniak.E, And McDermott.D., “Introduction to Artificial intelligence”, Addison-Wesley, 1987
2. Giarratano.J., And Riley G., ”Expert Systems principles an Programming” PWS-KENT,1989

REFERENCES:

1. Introduction to expert systems by Peter Jackson, 3rd edition, Addison-Wesley, 1999.
2. Expert systems: Principles and Programming, by Joseph C.Giarrantano, Gary D.Riley, Gary Riley, 4th edition, Cengage learning, 2004.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) T 4 C 4

(D0609151) VLSI TECHNOLOGY

(ELECTIVE II/MOOC)

(Common to DSCE, ES& PE)

UNIT I

INTRODUCTION TO MOS TECHNOLOGY & BASIC ELECTRICAL PROPERTIES OF MOS: Overview of VLSI Design Methodologies**,** VLSI Design flow, Styles of VLSI Design, CAD Technology, MOS Transistors and its Trends, I_{ds}-V_{ds} Relationships, Threshold voltage V_t, g_m, g_{ds} and W_o, Pass Transistor, MOS Z_{pu}/Z_{pd}, MOS Transistor circuit model.

UNIT II

CMOS DESIGN: CMOS Logic, Static Complementary gates, Transmission Gate Logic Design, Bi-CMOS Inverters, Latch-up in CMOS circuits.

UNIT III

LAYOUT DESIGN AND TOOLS:, Switch Logic, Alternative Gate Circuits, Transistor structures, Wires and Vias, Scalable Design rules, Layout Design tools.

UNIT IV

COMBINATIONAL LOGIC NETWORKS & INTERCONNECTS: Layouts, Simulation, Network Delay, Interconnect Design, Power Optimization, Switch Logic Networks, Gate and Network Testing.

UNIT V

SEQUENTIAL SYSTEMS: Memory Cells and Arrays, Clocking Disciplines, Design, Power Optimization, Design Validation and Testing.

UNIT VI

FLOOR PLANNING & ARCHITECTURE DESIGN: Floor Planning Methods, Off-Chip Connections, Architecture for Low Power, SOCs and Embedded CPU Architecture Testing.

TEXT BOOKS:

1. K. Eshraghian etal.(3 authors), “Essentials of VLSI Circuits and Systems”, PHI of India Ltd., 2005
2. Wayne Wolf, “Modern VLSI Design”, 3/E, Pearson Education, fifth Indian Reprint, 2005.
3. Sung-Mo Kang and Yusuf Leblebici, “CMOS Digital Integrated Circuits Analysis and Design” TATA McGraw Hill,3rdEdition, 2003.

REFERENCES:

1. N.H.E Weste, K.Eshraghian, “Principals of CMOS Design”, Addison Wesley, 2nd Edition.
2. Ken Martin, “Digital Integrated Circuits Design” oxford University Press, 2nd impression, 2005.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) T 4 C 4

(D0610151) ALGORITHMS FOR VLSI DESIGN AUTOMATION

(ELECTIVE II/MOOC)

(Common to DSCE & ES)

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT IV

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT V

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT VI

PHYSICAL DESIGN AUTOMATION OF MCM'S: MCM technologies, MCM physical design cycle, Partitioning, Placement - Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1) S.H.Gerez, "Algorithms for VLSI Design Automation", Wiley Student Edition, John Wiley& Sons (Asia) Pvt. Ltd., 1999.
2) NaveedSherwani, "Algorithms for VLSI Physical Design Automation", 3rd edition, Springer International Edition, 2005.

REFERENCES:

1) Hill & Peterson, "Computer Aided Logical Design with Emphasis on VLSI", Wiley, 1993.
2) Wayne Wolf, "Modern VLSI Design: Systems on silicon", Pearson Education Asia, 2nd Edition,1998.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) P C

3 2

(D5506151) MICROCONTROLLERS & INTERFACING LAB

8051 Microcontroller Assembly language Programs using 8051 kit.

1. Arithmetic operation –8-bit Addition and Subtraction, Multiplication and Division – Signed and unsigned Arithmetic operation.
2. Bubble Sorting.
3. Timer in different modes and applications S/W generation using delay.
4. Write a program to generate a train of pulses with different duty cycles.
5. Reading and writing a parallel port.
6. To count external pulses.

Interfacing programs.

1) Elevator Interface.
2) Key Board Interface.
3) Stepper motor interface
4) Traffic light controller
5) ADC
6) DAC
7) 7-Segment Display.
8) Serial communication interface.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, I-Sem (ES) P C

3 2

(D0611151) FPGA/CPLD LAB

(Common to DSCE & ES)

Minimum of 10 experiments to be conducted

1. Simulation and Verification of Logic Gates.
2. Simulation and Verification of 74x138.
3. Simulation and Verification of 74x151.
4. Simulation and Verification of 74x157.
5. Simulation and Verification of 74x280.
6. Simulation and Verification of 74x148.
7. Simulation and Verification of 74x74.
8. Simulation and Verification of 74x94.
9. Simulation and Verification of 74x163.
10. Simulation and Verification of 74x194.
11. Design, Simulation of Counters- Ring Counter, Johnson Counter, Mod counters.
12. Design, Simulation and verification of Dual Priority encoder.
13. Design, Simulation and verification of Floating point encoder.

Implementation of all the Design using FPGA and CPLD Devices.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) T 4 C 4

(D5508152) EMBEDDED SYSTEMS DESIGN

UNIT I

Embedded Design Life Cycle: Introduction, Product Specification, Hardware/software partitioning, Iteration and Implementation, Detailed hardware and software design, Hardware/Software integration, Product Testing and Release, Maintaining and upgrading existing products.

UNIT II

Selection Process: Packaging the Silicon, Adequate Performance, RTOS Availability, Tool chain Availability, Other issues in the Selection process, partitioning decision: Hardware/Software Duality, Hardware Trends, ASICs and Revision Costs.

UNIT III

Development Environment: The Execution Environment, Memory Organization, System Startup. Special Software Techniques: Manipulating the Hardware, Watchdog Timer, Flash Memory, Design Methodology. Basic Tool Set: Host – Based Debugging, Remote Debuggers and Debug Kernels, ROM Emulator, Logic Analyzer.

UNIT IV

BDM: Background Debug Mode, Joint Test Action Group (JTAG) and Nexus. ICE – Integrated Solution: Bullet Proof Run Control, Real time trace, Hardware Break points, Overlaymemory, Timing Constrains, Usage Issue, Setting the Trigger.

UNIT V

Testing: The role of testing in embedded systems,Choosing Test cases, Testing Embedded Software, Performance Testing Maintenance and Testing.

Debugging techniques: Debugging techniques, the role of the development system.

UNIT VI

Writing Software for Embedded Systems: The compilation Process,Native Versus Cross-Compilers, Runtime Libraries, Writing a Library, Using alternative Libraries, using a standard Library.

TEXTBOOKS

1. Embedded System Design – Introduction to Processes, Tools, Techniques, Arnold S Burger, CMP Books , 2002.
2. Embedded Systems Design by Steve Heath, Newnes, 2nd edition 2003, EDN series for design engineers.

REFERENCES:

1. An embedded software primer by David E.Simon, Pearson education, 2008, Low price edition.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) T 4 C 4

(D5509152) REAL TIME OPERATING SYSTEMS

UNIT-I

REAL TIME OPERATING SYSTEMS: Architecture of kernel, Tasks and Task scheduler, Task States, Context Switching, Scheduling Algorithms, Rate Monotonic Analysis, Task Management Call Functions, Interrupt services routines, Semaphores, Mutex, Mailboxes, Message queues, Event register, Pipes, Signals, Timers, Memory management, Priority inversion problem, Priority Inheritance, Path Finder Problem Revisited.

UNIT-II

REAL TIME APPLICATIONS: : Digital control, Selection of sampling period, Multirate Systems, Example of software controlled systems, Timing characteristics, Complex control law computations, Kalman filter, High level controls, Control hierarchy ,Guidance and control, Timing requirements, Real time command and Control, signal processing, Radar systems, other real time applications.

UNIT-III

HARD VERSUS SOFT REAL TIME SYSTEMS: Jobs and processors, release times, deadlines, and timing constraints. Hard and soft timing constraints.Hard real time systems, soft real time systems.

REAL TIME SCHEDULING APPROACHES: Clock Driven, Weighted round robin, priority driven, dynamic vs static systems, effective release times andead lines.

UNIT-IV

REAL TIME OPERATING SYSTEM: QNX Neutrino, VX works, Microc/os-II, RT Linux, overview of unix/Linux.

SHELL AND SYSEM PROGRAMMING: Shell programming-shell variables, shell programming constructs, processes, signals, multithreading, semaphores, mutex, shared memory, messagequeue.

UNIT-V

PROGRAMMING IN RT LINUX: Overview of RT Linux, core RT Linux API, semaphore management, mutex management.

UNIT-VI

FAULT TOLERANCE TECHNIQUES: Introduction, fault causes, Types, detection, Fault and error containment, Hardware, software and timing redundancy

TEXTBOOKS

1) Embedded Real Time Systems-BlackbookDr.K.V.K.K.Prasad, 2005 edition, Dreamtech press.
2) Jane W.S.Liu,"Real Time Systems",Pearson education, 2007.
3) C.M.Krishna,KANGG.Shin,"Real Time Systems",McGraw Hill, 1997.

REFERENCES

1) www.kernel.org.
2) Vxworks Programming Guide.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) T 4 C 4

(D5510152) HARDWARE SOFTWARE CO-DESIGN

UNIT I

CO- DESIGN ISSUES: Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

HARDWARE/SOFTWARE CO- SYNTHESIS ALGORITHMS: Introduction, preliminaries, Architectural model hardware – software partitioning, distributed system co-synthesis.

UNIT II

PROTOTYPING AND EMULATION: Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping, system communication infrastructure

UNIT III

TARGET ARCHITECTURES: Architecture Specialization techniques, Target Architecture and Application System classes, Architecture for control dominated systems (8051-Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), and Mixed Systems.

UNIT IV

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern embedded architectures, embedded software development needs, compilation technologies practical consideration in a compiler development environment.

UNIT V

DESIGN SPECIFICATION AND VERIFICATION: Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, and interface verification

UNIT VI

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN: System – level specification, design representation for system level synthesis, system level specification languages, Heterogeneous specifications and multi-language co-simulation.

TEXT BOOKS:

1. Jorgen Staunstrup, Wayne Wolf, “Hardware / software co- design Principles and Practice”,
2. Springer, 2009.
3. Kluwer, “Hardware / software co- design Principles and Practice”, academic publishers,2002.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) T 4 C 4

(D0618152) EMBEDDED 'C'

(Common to DSCE & ES)

UNIT I

PROGRAMMING EMBEDDED SYSTEMS IN C: Introduction to embedded system, Processor used, programming language used, operating system used, developing embedded software.

INTRODUCING THE 8051 MICROCONTROLLER FAMILY: Introduction, The external interface of the Standard 8051, Reset requirements, Clock frequency and performance Memory issues, I/O pins, Timers, Interrupts, Serial interface, Power consumption.

UNIT II

EMBEDDED WORLD: Introduction Installing the Keil software and loading the project, Configuring the simulator, Building the target, Running the simulation, Dissecting the program, Building the hardware.

UNIT III

READING SWITCHES: Introduction, Basic techniques for reading from port pins, Example: Reading and writing bytes, Example: Reading and writing bits (simple version),The need for pull-up resistors, Dealing with switch bounce, Example: Reading switch inputs (basic code).

UNIT IV

ADDING STRUCTURE TO YOUR CODE: Introduction, Object-oriented programming with C, The Project Header (MAIN.H), The Port Header (PORT.H), Example: Restructuring the 'Hello Embedded World' example.

UNIT V

MEETING REAL-TIME CONSTRAINTS: Introduction, Creating 'hardware delays' using Timer 0 and Timer, Example: Generating a precise 50 ms delay, Example: Creating a portable hardware delay, The need for 'timeout' mechanisms, Creating loop timeouts.

UNITVI

CREATING AN EMBEDDED OPERATING SYSTEM: Introduction, The basis of a simple embedded OS, Introducing sEOS, Using Timer 0 or Timer 1, alternative architectures, important design considerations when using sEOS.

MULTI-STATE SYSTEMS AND FUNCTION SEQUENCES: Introduction, Implementing a Multi-State (Timed) system, traffic light sequencing, Animatronics dinosaur, implementing a Multi-State (Input/Timed) system, Controller for a washing machine

TEXT BOOKS:

1. Embedded C By Micheal J. Pont Pearson Education, 2002.
2. Embedded C Coding standard-Michael Barr from Neutrino.

REFERENCES:

1. Real Time Concepts for Embedded systems-Qing Li,Caroline Yao, CMP Books 2003.
2. Embedded/Real Time Syatems-KVKK Prasad,Dreamtech press,2005.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) T 4 C 4

(D5511152) CMOS DIGITAL IC DESIGN

(ELECTIVE-III)

UNIT I

MOS Transistor: MOS Structure, MOS System under external bias, Structure and operation of MOSFET, Threshold voltage, MOSFET operation: A qualitative view. MOSFET Current-voltage characteristics: Gradual channel approximation, Channel length modulation, Substrate bias effect.

UNIT II

Constant field scaling, Constant voltage scaling, short channel effects, Narrow channel effects. MOSFET Models and Capacitance: Oxide-related capacitance, Junction capacitance. Level1, Level2, Level 3 modeling equations.

UNIT III

CMOS Inverter: Circuit operation, calculation of $V_{IL,}$ $V_{IH,}V_{th.}$ Design of CMOS inverters, Supply scaling in CMOS inverter, Power and area considerations.

UNIT IV

CMOS Inverter switching characteristics: Delay-time definition, calculation of delay times, Inverter design with delay constraints. Estimation of Interconnects parasitic: Interconnect capacitance estimation, Interconnect resistance estimation. Calculation of Interconnect delay: RC delay Models, The Elmore delay.

UNIT V

Sequential MOS logic circuits: Behavior of Bi-stable elements, SR Latch circuit, Clocked SR latch, Clocked JK Latch, Master-Slave flip-flop, CMOS D-Latch and Edge-Triggered Flip-Flop.

UNIT VI

Low Power CMOS logic circuits: Switching power dissipation, Short-circuit power dissipation, Leakage power dissipation, Influence of voltage scaling on Power and delay, Variable-Threshold CMOS (VTCMOS) circuits, Multiple-Threshold CMOS(MTCMOS) circuits, Pipeline approach, Parallel processing approach(Hardware replication).

TEXT BOOKS:

1. Sung-Mo Kang & Yusuf Leblebici, “CMOS Digital Integrated Circuits - Analysis &Design”, MGH, Second Ed., 1999.
2. Jan M Rabaey, “Digital Integrated Circuits - A Design Perspective”, Prentice Hall, 1997.

REFERENCES:

1. Eugene D Fabricus, “Introduction to VLSI Design,”McGraw Hill International Edition.1990.
2. R. J. Baker, H. W. Li, and D. E. Boyce, “CMOS circuit design, layout, and simulation”. New York: IEEE Press, 1998.
3. Ken Martin, “Digital Integrated Circuit Design”, Oxford University Press, 2000.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) T 4 C 4

(D0620152) NETWORK SECURITY AND CRYPTOGRAPHY

(ELECTIVE-III)

(Common to DSCE & ES)

OBJECTIVES:

1. To study various aspects of Network Security Attacks, Services and Mechanisms.
2. To understand the mathematical concepts of various Encryption, Authentication and Digital Signature Algorithms.
3. To standby the design of different general purpose and application specific security Protocols and standards.
4. To identify suitable points for applying security features for network traffic

OUTCOMES:

1. The students will be able to understand and implement various public and private key cryptographic algorithms.
2. The student will be able to protect the system and network from various attacks.
3. The student will be able to design new security approach

UNIT-I

INTRODUCTION: Computer Security Concepts, The OSI Security Architecture, Security Services, Mechanisms, Attacks, Network Security Model, Classical Encryption Techniques – Symmetric Cipher Model, Substitution Techniques, Transposition Techniques, Rotor Machines, Steganography.

BLOCK CIPHERS AND DATA ENCRYPTION STANDARD: Block Cipher Principles, Stream Ciphers and Block Ciphers, Feistel Cipher Structure , Data Encryption Standard, DES Example, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles, AES..

UNIT II

PUBLIC-KEY CRYPTOSYSTEMS: Principles Of Public-Key Cryptosystems, RSA Algorithm, Diffie-Hellman Key Exchange, Elliptic Curve Arithmetic, Elliptic Curve Cryptography, PRNG Based on RSA, PRNG Based on Elliptic Curve Cryptography.

UNIT III

CRYPTOGRAPHIC HASH FUNCTIONS:Applications of Cryptographic Hash functions, Requirements and security, Hash functions based on Cipher Block Chaining, Secure Hash Algorithm (SHA-1), Message authentication Requirements.

MESSAGE AUTHENTICATION CODES: Message authentication functions, Requirements for Message authentication codes, security of MACs, HMAC, MACs based on Block Ciphers, Authenticated Encryption.

UNIT IV

DIGITAL SIGNATURES:Digital Signatures, Digital Signatures Properties, Attacks and Forgeries, Digital Signature Requirements, Direct Digital Signature, Digital Signature Standard, DSS Approach, Digital Signature Algorithm.

KEY MANAGEMENT AND DISTRIBUTION: Symmetric key distribution using Symmetric Encryption, Symmetric key distribution using Asymmetric, Distribution of Public keys, X.509 Certificates, Public key Infrastructure.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

UNIT V

USER AUTHENTICATION: Remote user Authentication Principles, Remote user Authentication using Symmetric Encryption, Kerberos, Remote user Authentication using Asymmetric Encryption, Federated Identity Management

ELECTRONIC MAIL SECURITY: Pretty Good Privacy (PGP), S/MIME

UNIT VI

SECURITY AT THE TRANSPORT LAYER (SSL AND TLS) : SSL Architecture, Four Protocols, SSL Message Formats, Transport Layer Security, HTTPS, SSH

SECURITY AT THE NETWORK LAYER (IPSEC): Two modes, Two Security Protocols, Security Association, Security Policy, Internet Key Exchange.

SYSTEM SECURITY

Intruders, Intrusion Detection, Password Management, Types of Malicious Software, Viruses, Virus Countermeasures, Worms, Distributed Denial of Service Attacks, Firewalls.

TEXT BOOKS:

1. Cryptography and Network Security: Principals and Practice, William Stallings, Fifth Edition, Pearson Education.
2. Cryptography and Network Security, Behrouz A. Frouzan and Debdeep Mukhopadhyay, 2 nd edition, Mc Graw Hill Education.

REFERENCES:

1. Cryptography and Network Security, William Stallings, PHI, New Delhi, 2nd Edition, 1999
2. Cryptography and Security, C.K. Shymala, N. Harini and Dr. T.R. Padmanabhan, Wiley-India.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) T 4 C 4

(D5512152) ANALOG IC DESIGN

(ELECTIVE-III)

UNIT I

MOS transistors- modeling in linear, saturation and cutoff high frequency equivalent circuit.

UNIT II

INTEGRATED DEVICES AND MODELING AND CURRENT MIRROR: Advanced MOS Modeling, Large Signal and Small Signal Modeling for BJT/Basic Current Mirrors and Single Stage Amplifiers: Simple CMOS Current Mirror, Common Source, Common Gate Amplifier With Current Mirror Active Load. Source Follower with Current Mirror to Supply Bias Current, High Output Impedance Current Mirrors and Bipolar Gain Stages. Frequency Response.

UNIT III

OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION: Two Stage CMOS Operational Amplifier. Feedback and Operational Amplifier Compensation. Advanced Current Mirror. Folded–Cascade Operational Amplifier, Current Mirror Operational Amplifier Fully Differential Operational Amplifier. Common Mode Feedback Circuits. Current Feedback Operational Amplifier. Comparator . Charge Injection Error. Latched Comparator and Bi-CMOS Comparators.

UNIT IV

SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-I: MOS, CMOS, Bi-CMOS Sample and Hold Circuits. Switched Capacitor Circuits: Basic Operation and Analysis. First Order and Biquard Filters.

UNIT V

SAMPLE AND HOLD SWITCHED CAPACITOR CIRCUITS-II: Charge Injection. Switched Capacitor Gain Circuit. Correlated. Double Sampling Techniques. Other Switched Capacitor Circuits.

UNIT VI

DATA CONVERTERS: Ideal D/A & A/D Converters. Quantization Noise. Performance Limitations. Nyquist Rate D/A Converters: Decoders Based Converters. Binary Scaled Converters. Hybrid Converters. Nyquist Rate A/D Converters: Integrating, Successive Approximation, Cyclic Flash Type, Two Step, Interpolating, Folding and Pipelined, A/D Converters. Over Sampling With and Without Noise Shaping

TEXT BOOKS:

1. D.A.JOHN & KEN MARTIN: “Analog Integrated Circuit Design”. John Wiley, 1997.
2. Behzad Razavi, “Design of Analog CMOS Integrated Circuit” Tata-Mc GrawHill, 2002

REFERENCES:

1. Philip Allen & Douglas Holberg, “CMOS Analog Circuit Design”, Oxford University Press,2002
2. GREGOLIAN &TEMES: Analog MOS Integrated Circuits, John Wiley, 1986.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) T 4 C 4

(D0621152) SYSTEM MODELING AND SIMULATION

(ELECTIVE-IV/MOOC)

(Common to DSCE & ES)

UNIT I

Basic Simulation Modeling, Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT II

SIMULATION SOFTWARE: Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT III

BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

UNIT IV

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.
EXOGENOUS SIGNALS AND EVENTS: Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation.

UNIT V

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous-Time Markov processes.

UNIT VI

EVENT DRIVEN MODELS: Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple servers.
SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation mythology.

TEXTBOOKS

1. System Modeling & Simulation, An Introduction – Frank L. Severance, John Wiley & Sons, 2001.
2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

REFRENCE BOOKS

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) T 4 C 4

(D5513152) LOW POWER VLSI DESIGN

(ELECTIVE – IV/MOOC)

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II

MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration considerations.
Bi-CMOS Isolation considerations.

UNIT III

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS.

UNIT IV

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models,

UNIT V

Sub-half micron MOS devices: Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT VI

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.
LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

TEXT BOOKS:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl (3 Authors)-Pearson Education Asia 1st Indian reprint,2002.
2. Gary K. Yeap, “Practical Low Power Digital VLSI Design”, KAP, 2002.

REFERENCES:

1. Digital Integrated circuits, J.Rabaey PH. N.J 1996
2. CMOS Digital ICs Sung-mo Kang and yusufleblebici 3rd edition TMH 2003 .

IEEE Trans Electron Devices, IEEEJ.SolidState Circuits, and other National and International Conferences and Symposia.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) T 4 C 4

(D0623152) FPGA ARCHITECTURE & APPLICATIONS

(ELECTIVE – IV/MOOC)

(Common to DSCE & ES)

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, FPGA – Features, Complex Programmable Logic Devices: ALTERA CPLDs and ALTERA FLEX 10k Series CPLD, Speed Performance.

FPGA: Xilinx logic Cell array, CLB,I/O Block Programmable interconnect, Technology Mapping for FPGA: Library based, LUT based, Multiplexer based Technology Mapping.

UNIT II

CASE STUDIES: programming Technologies, Xilinx XC3000, XC4000, Actel FPGAs, Alteras FPGAs, Plus Logic FPGA, AMD FPGA, Quick Logic FPGA, Algotronix FPGA, Cross point solutions FPGA, FPGA Design Flow.

UNIT III

FINITE STATE MACHINES (FSM): Finite State Machine– State Transition Table, State Assignments for FPGAs. Problem of the Initial State Assignment for One Hot Encoding.

REALIZATION OF STATE MACHINE: Derivation of SM Charts. Realization of State Machine Chart, Alternative Realization of State Machine Chart using Microprogramming. Linked State Machines. One–Hot State Machine,

UNIT IV

FSM ARCHITECTURES: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around A Shift Register. Petri nets for State Machines – Basic Concepts, Properties. Extended Petri nets for Parallel Controllers.

UNIT V

SYSTEMS LEVEL DESIGN: One–Hot Design Method. Use of ASMs in One–Hot Design. Application of One–Hot Method. System Level Design: Controller, Data Path and Functional Partition.

UNIT VI

DIGITAL FRONT END DIGITAL DESIGN FOR FPGAS & ASIC: Using Xilinx ISE EDA Tool Guidelines, Case Studies of Parallel Adder Cell, Parallel Adder, Sequential Circuits: Decade Counters, Parallel Multipliers, Parallel Controllers.

TEXT BOOKS:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, Prentice Hall (Pte), 1994.
2. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.

REFERENCES:

1. Fundamentals of logic Design, 5/e, Charles H Roth.Jr.
2. S. Brown, R. Francis, J. Rose, Z. Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.
3. Engineering Digital Design, 2/e, Richard F Tinder **Unit VI & VII**.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) P C

3 2

(D0624152) EMBEDDED SYSTEMS PROGRAMMING LAB

(Common to DSCE & ES)

Embedded C programming and testing using 8051 advanced development board and KEIL tools.

1. (i) Program to perform arithematic operations.
   (ii) Program to perform sorting of numbers.
2. Program to shift LED's Left and right.
3. Program for DIP switch interface.
4. Program to display message in LCD 8 bit mode.
5. Program to display picture in GLCD 128X64.
6. Program to send data serially through serial port.
7. Program to display I2C RTC(DS1307) to Hyper terminal window.
8. Program to display digital temperature sensor output.
9. Program for 4X4 matrix keyboard with LCD.
10. (i)Program to interface stepper motor.
11. (ii)Program to interface relay.

Embedded C programming and testing using LPC2148 development kit(Real time environment)

1. Program to interface LED and implement Multi-tasking.
2. Program to display RTC-ADC on LCD.
3. Program to display message on GLCD.

RAJEEV GANDHI MEMORIAL COLLEGE OF ENGINEERING AND TECHNOLOGY

Autonomous

EMBEDDED SYSTEMS

M.Tech, II-Sem (ES) P C

3 2

(D5514152) CMOS DIGITAL IC DESIGN LAB

Minimum of 10 experiments to be conducted

Design and Analysis of CMOS based functions using Layouts.

1. INVERTER
2. AND
3. NAND
4. OR
5. NOR
6. XOR
7. XNOR
8. HALF ADDER
9. SR-LATCH
10. 1-BIT COMPARATOR
11. D-LATCH
12. BUFFER