(12) PATENT APPLICATION PUBLICATION(19) INDIA

(19) INDIA

(22) Date of filing of Application :26/06/2021

(43) Publication Date : 09/07/2021

(54) Title of the invention : COMPUTATIONAL OPTIMIZATION OF VLSI PHYSICAL DESIGN WITH GRAPHICAL PROCESSING UNITS ISING METHOD

 (51) International classification (31) Priority Document No (32) Priority Date (33) Name of priority country (86) International Application No Filing Date (87) International Publication No (61) Patent of Addition to Application Number Filing Date (62) Divisional to Application Number Filing Date 	:G06N001000000, G06N0007000000, G06F0017110000, G06F0017100000 :NA :NA :NA :NA :NA :NA :NA :NA :NA :NA	 (71)Name of Applicant : ()B. Eshwar, Assistant Professor/ Department of ECE, Lords Institute of Engineering & Technology Address of Applicant :Lords Institute of Engineering & Technology, Himayath Sagar, Hyderabad, Telangana-500091. Telangana India 2)M. Maheswari, Assistant Professor/ Department of ECE, RGMCET. 3)Dr.T.Nageswara Rao, Associate Professor/ Department of Mathematics, Koneru Lakshmaiah Education Foundation. 4)Dr.G.N.V.Kishore, Associate Professor/ Department of Engineering Mathematics and Humanities, SRKR Engineering College. 5)Dr. S.M. Chithra, Associate Professor/ Department of Mathematics, RMK College of Engineering and Technology 6)Dr.T. Surendra, Assistant Professor/Department of Mathematics, GITAM Deemed University 7)Valamiki Saraswathi, Assistant Professor/Department of ECE, RGMCET. (?2)Name of Inventor : 1)B. Eshwar, Assistant Professor/Department of ECE, RGMCET. 3)Dr.T.Nageswara Rao, Associate Professor/ Department of ECE, RGMCET. 3)Dr.T.Nageswara Rao, Associate Professor/Department of ECE, RGMCET. 3)Dr.T.Nageswara Rao, Associate Professor/ Department of ECE, RGMCET. 3)Dr.T.Nageswara Rao, Associate Professor/Department of ECE, RGMCET. 3)Dr.T.Nageswara Rao, Associate Professor/Department of ECE, RGMCET. 3)Dr.T.Nageswara Rao, Associate Professor/Department of ECE, RGMCET. 3)Dr.S.M. Chithra, Associate Professor/Department of Anthematics, RMK College of Engineering and Technology 6)Dr. S.M. Chithra, Associate Professor/Department of Mathematics, RMK College of Engineering and Technology 6)Dr. T. Surendra, Assistant Professor/Department of Mathematics, GITAM Deemed University 7)Valamiki Saraswathi, Assistant Professor/Department of Mathematic
---	---	--

(57) Abstract :

Abstract Many VLSI physical design techniques, such as maximum cut and maximum flow, have significantly more difficult solutions to design, compute, and prove. This domain's extensive elements make certain issues computationally impossible, and as a result, approximate solutions are necessary. Here, we take the Ising spin glass model, a computational approach useful for hard combinatorial optimization problems, and apply it to specific hard combinatorial optimization problems. In the Ising model, ferromagnetism is represented as a mathematical model in statistical mechanics. According to this theorem, while applying the Ising computing technique, a minimal energy state is found for the Ising model, which approximates the expected optimal solution to the original problem. Mapping combinatorial optimization issues into the Ising model is quite popular in combinatorial optimization research. While we're in the VLSI physical design industry, we specialize in the max-cut problem because it's important to numerous difficulties inside that field. While investigating the behavior of the Ising annealing process, we found that the procedure is well-suited to parallel GPU computing massively. Using GPU random thread scheduling shows how to construct random update patterns that improve GPU resource consumption. FPGA- and other hardware-based implementation approaches were demonstrated to be inadequate regarding the rigour required in creating an Ising graph. For a set of demanding optimization methods, proposed GPU implementation delivers more than 2000X speedup over CPU implementation.

No. of Pages : 13 No. of Claims : 5