(12) PATENT APPLICATION PUBLICATION
(19) INDIA
(22) Date of filing of Application :15/07/2021

(21) Application No.202141031941 A
(43) Publication Date : 23/07/2021

(54) Title of the invention : Low Power VLSI Implementation of Multi-Layer Neural Networks

(51) International classification	:G06N0003040000, G06N0003063000, G06F0030367000, H01L0023538000, G11C0013040000
(31) Priority Document No	:NA
(32) Priority Date	:NA
(33) Name of priority country	:NA
(86) International Application No Filing Date	:PCT// :01/01/1900
(87) International Publication No	: NA
(61) Patent of Addition to Application Number Filing Date	:NA :NA
(62) Divisional to Application Number Filing Date	:NA :NA

(71)**Name of Applicant :**
1)Easari. Parusha Ramu, Assistant Professor/ Department of ECE
Address of Applicant :Sri Indu College of Engineering & Technology (Autonomous), Ibrahimpatnam, R.R. District, Telangana-501510 Telangana India
2)Prathyusha. V, Assistant Professor/ Department of ECE
3)B. Srinivasa Kumar, Associate Professor/ Department of Mathematics
4)V. Sunitha, Assistant Professor/ Department of ECE.
5)Pologoni Srinivas, Assistant Professor/ Department of ECE
6)Dr.V Sandeep Kumar, Assistant Professor / Department of ECE
7)Dr. J. Sofia Priya Dharshini, Associate Professor / Department of ECE.
8)Swathi Singanaboina, Assistant Professor/ Department of ECE
(72)**Name of Inventor :**
1)Easari. Parusha Ramu, Assistant Professor/ Department of ECE
2)Prathyusha. V, Assistant Professor/ Department of ECE
3)B. Srinivasa Kumar, Associate Professor/ Department of Mathematics
4)V. Sunitha, Assistant Professor/ Department of ECE.
5)Pologoni Srinivas, Assistant Professor/ Department of ECE
6)Dr.V Sandeep Kumar, Assistant Professor / Department of ECE
7)Dr. J. Sofia Priya Dharshini, Associate Professor / Department of ECE.
8)Swathi Singanaboina, Assistant Professor/ Department of ECE

(57) Abstract :
Abstract An integrate-and-fire-type spiking neuron model is proposed, which is based on a time-domain analogue weighted-sum computation model. In feed-forward neural networks, summations with positive and negative weights are computed individually in each layer. The results are then passed into the next layers without any subtraction step. To complement the proposed model, we additionally propose large-scale integrated (VLSI) circuits. The time-domain analogue circuits use transient operation for charging and discharging processes, unlike conventional analogue voltage or current mode circuits. It is possible to design circuits without operational amplifiers, which means they consume less. Nonetheless, they must use high resistance devices with a resistivity greater than GÎ. To test weighted-sum operation with the same weights, we created a proof-of-concept (POC) CMOS VLSI chip and simulated it using post-layout circuit modelling utilizing 250-nm fabrication technology. With the MOS transistor sub-threshold operation area, it was possible to achieve a high resistance operation. Despite connectivity width requirements of at least two orders of magnitude higher in digital AI processors, simulation findings indicated that weighted-sum computation efficiency was over 290 TOPS/W, well over one order of magnitude greater than the state-of-the-art digital AI processing units. For this proposed concept, if cutting-edge VLSI technology is applied, a TOPS/W energy efficiency of above 1,000 is feasible. Such developing analogue memory devices, such as ferroelectric-gate FETs, are needed for practical applications.

No. of Pages : 13 No. of Claims : 3

FORM - 2

THE PATENTS ACT, 1970

(39 OF 1970)

THE PATENTS RULES, 2003

COMPLETE SPECIFICATION

(Section 10; rule 13)

Low Power VLSI Implementation of Multi-Layer Neural Networks

Easari. Parusha Ramu, Assistant Professor/ Department of ECE.	**Sri Indu College of Engineering & Technology (Autonomous), Ibrahimpatnam, R.R. District, Telangana-501510.**
Prathyusha. V, Assistant Professor/ Department of ECE.	**Sri Indu College of Engineering & Technology (Autonomous), Ibrahimpatnam, R.R. District, Telangana-501510.**
B. Srinivasa Kumar, Associate Professor/ Department of Mathematics.	**Koneru Lakshmaiah Education Foundation, Vaddeswaram, Guntur, A.P-522502.**
V. Sunitha, Assistant Professor/ Department of ECE.	**Sri Indu College of Engineering & Technology (Autonomous), Ibrahimpatnam, R.R. District, Telangana-501510.**
Polagoni Srinivas, Assistant Professor/ Department of ECE.	**Sri Indu College of Engineering & Technology (Autonomous), Ibrahimpatnam, R.R. District, Telangana-501510.**
Dr.V Sandeep Kumar, Assistant Professor / Department of ECE.	**Samskruti College of Engineering and Technology, Ghatkesar, Kondapur, Medchal, Hyderabad, Telangana-501301.**
Dr. J. Sofia Priya Dharshini, Associate Professor / Department of ECE.	**Rajeev Gandhi Memorial College of Engineering and Technology, Nandyal, Kurnool, A.P-518501.**
Swathi Singanaboina, Assistant Professor/ Department of ECE.	**Sri Indu College of Engineering & Technology (Autonomous), Ibrahimpatnam, R.R. District, Telangana-501510.**

The following specification particularly describes the invention and the way it is to be performed: